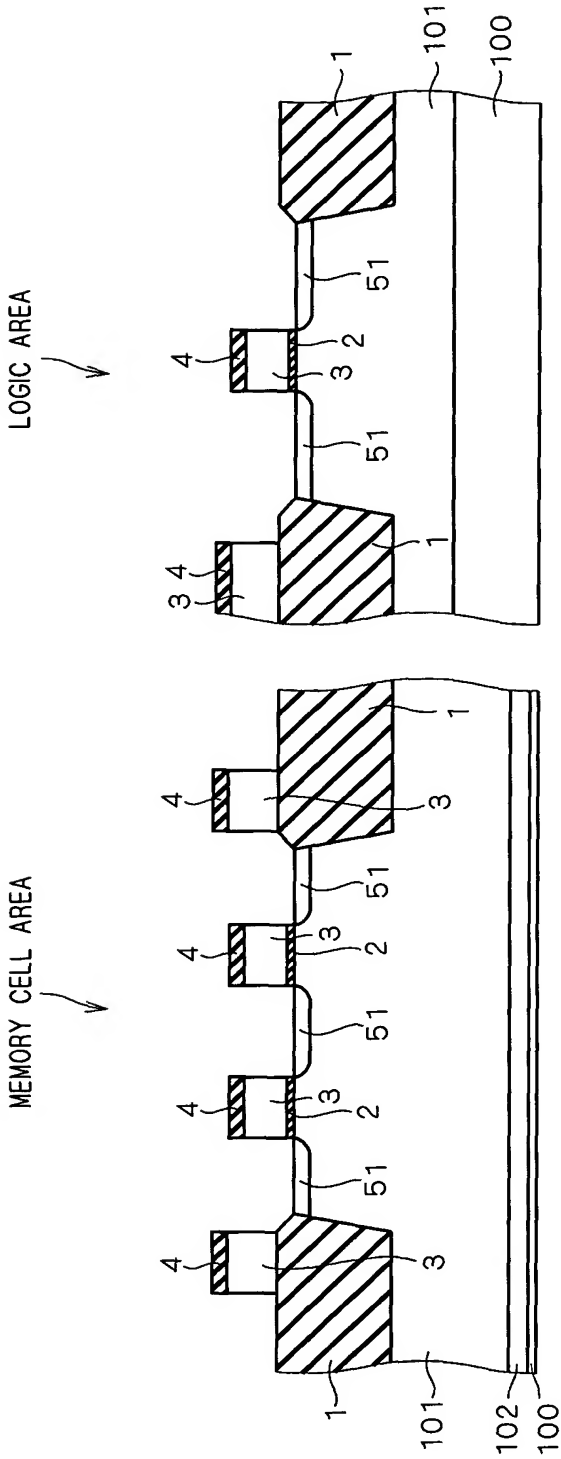


F I G . 1



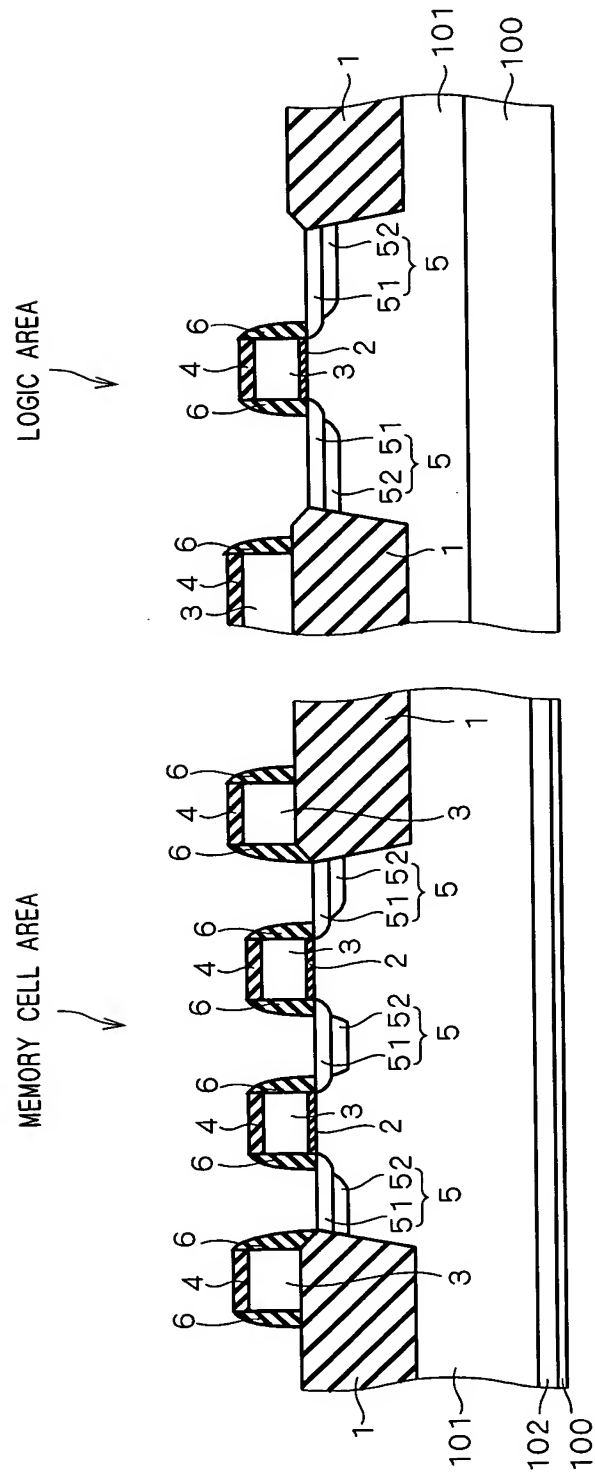
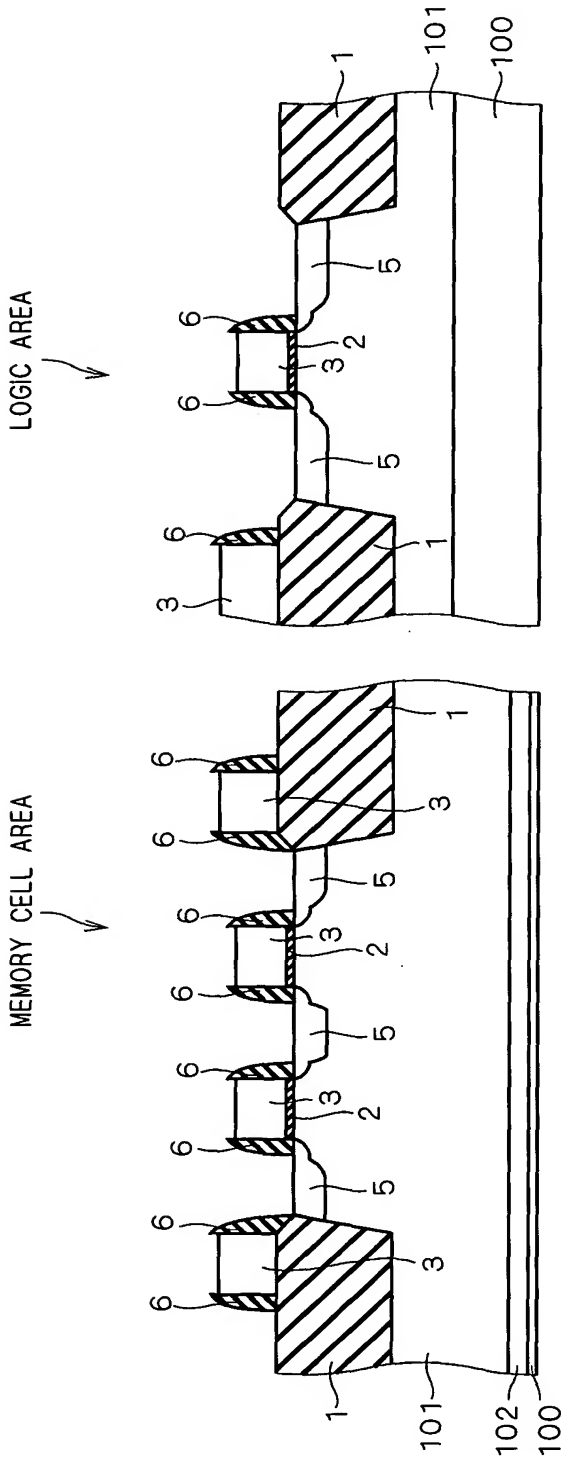
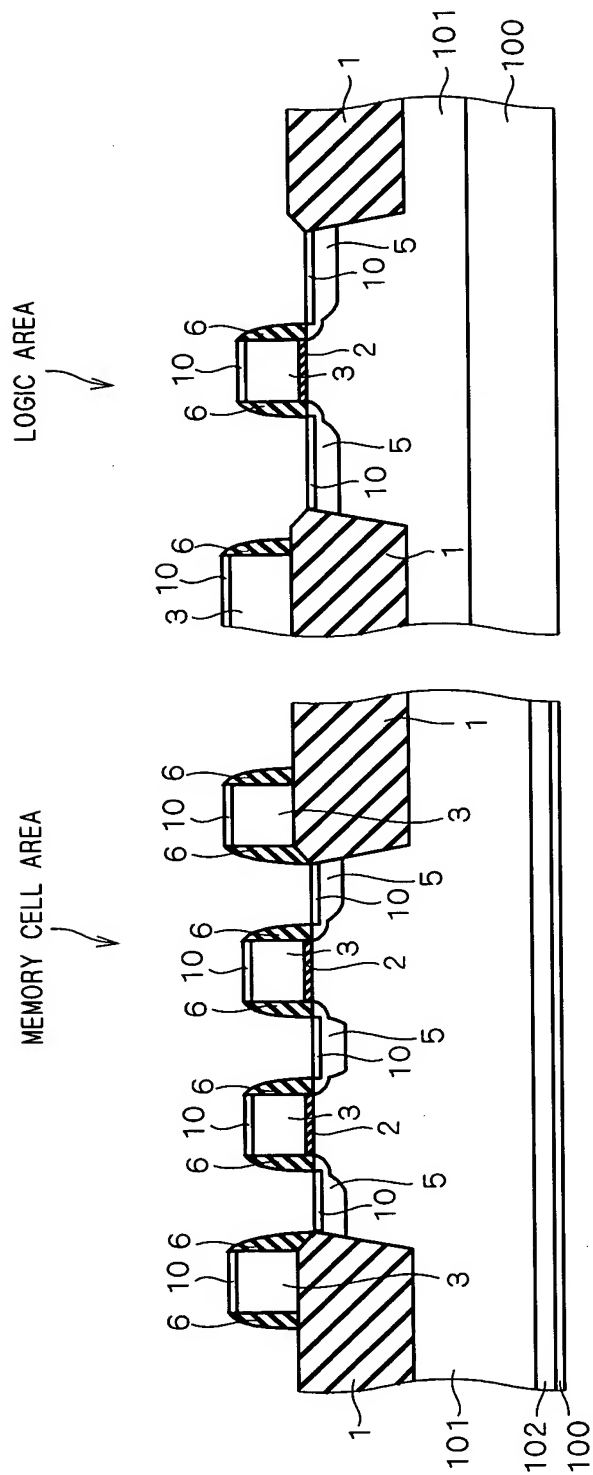


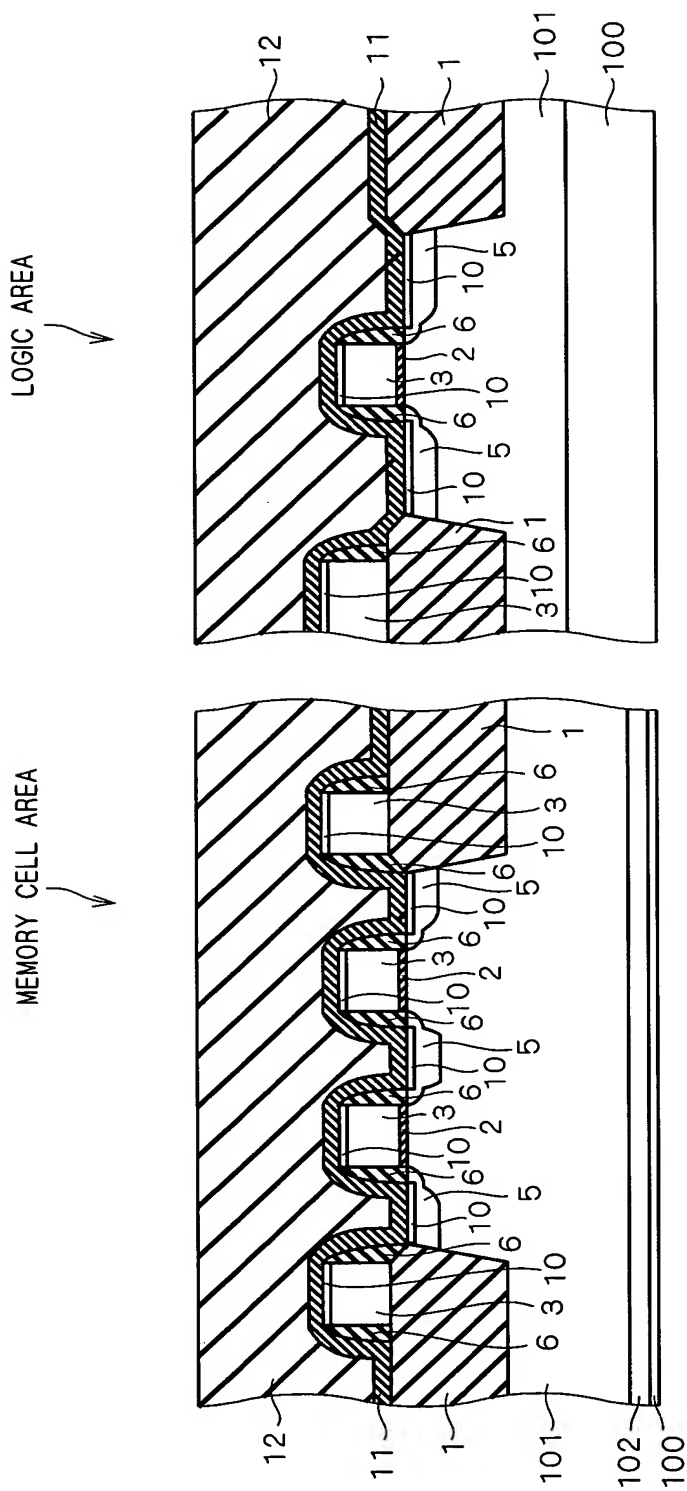
FIG. 3



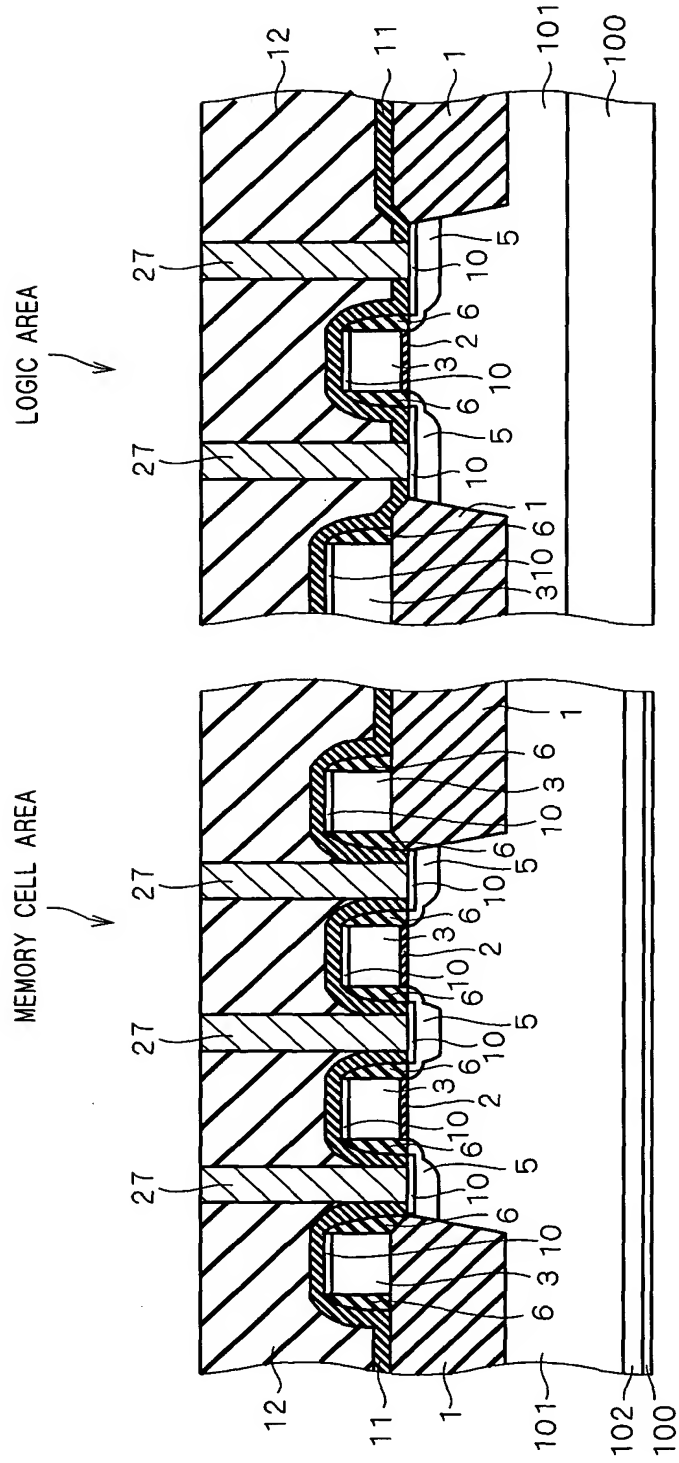
F I G . 4



F I G . 5



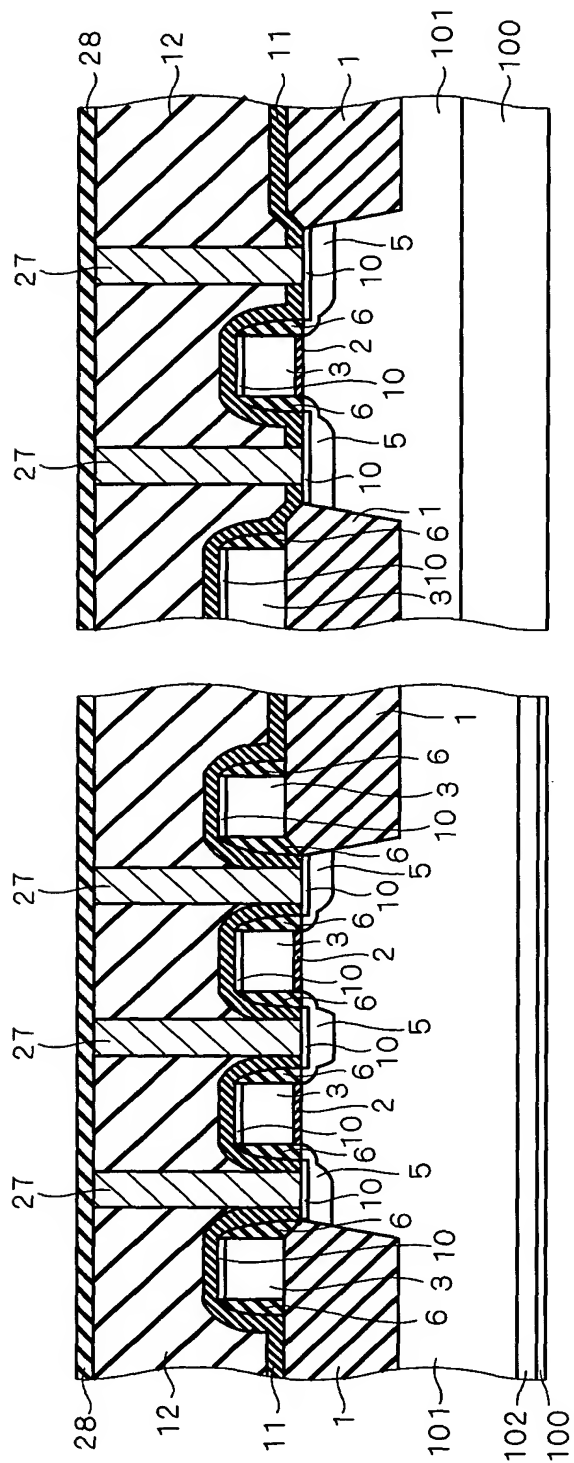
F I G . 6



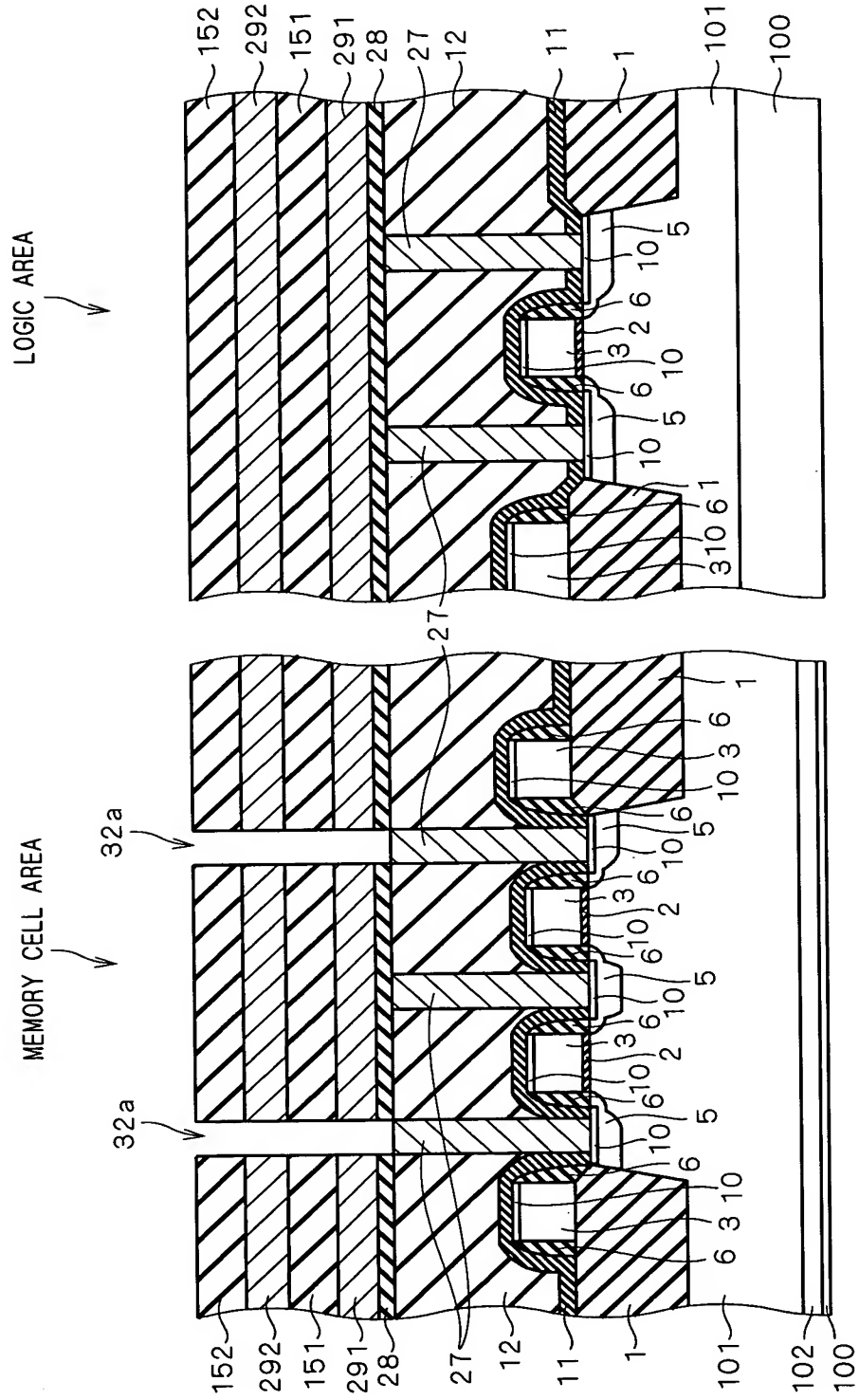
F I G . 7

MEMORY CELL AREA

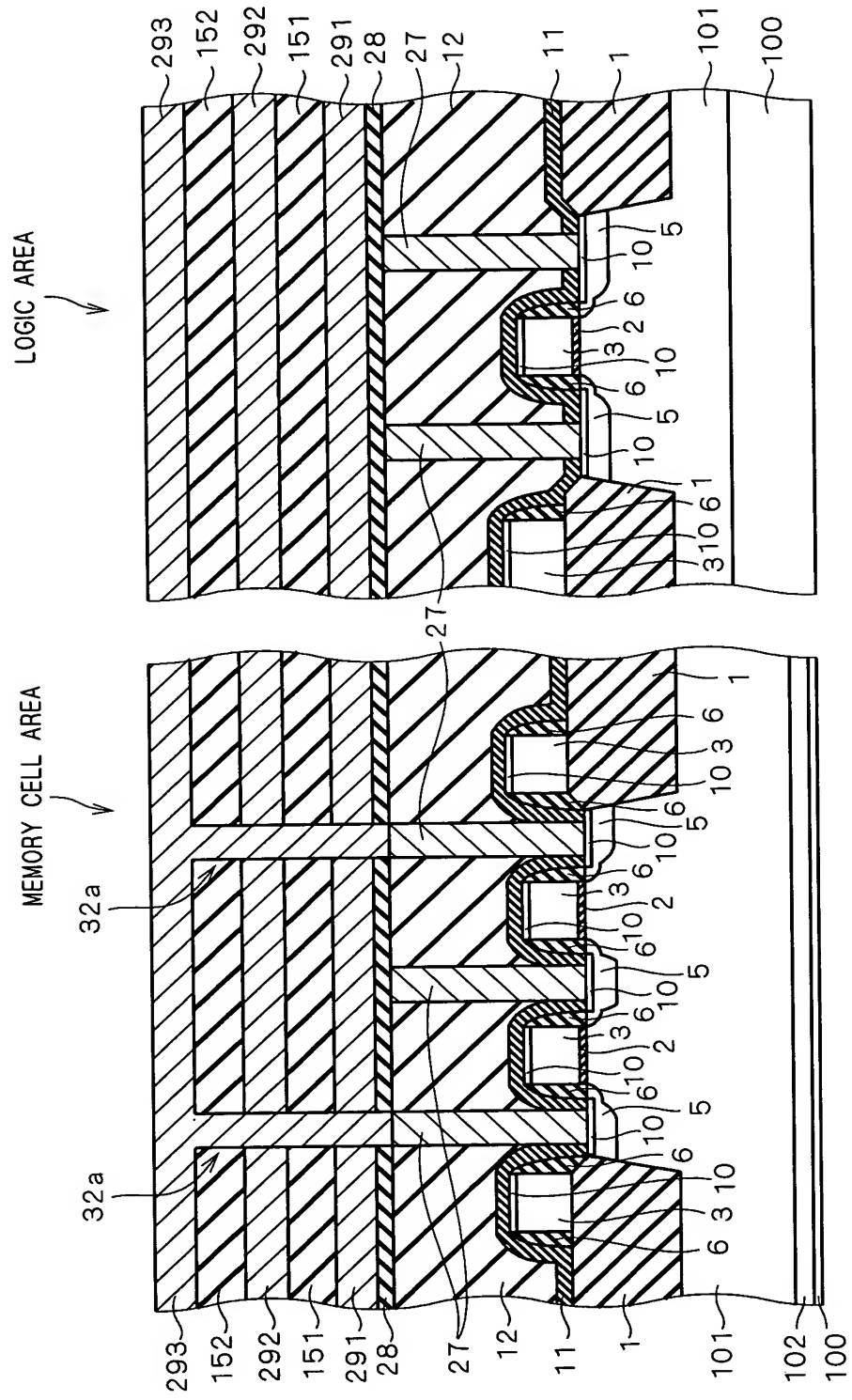
LOGIC AREA



F I G . 8



F I G . 9



F I G . 1 0

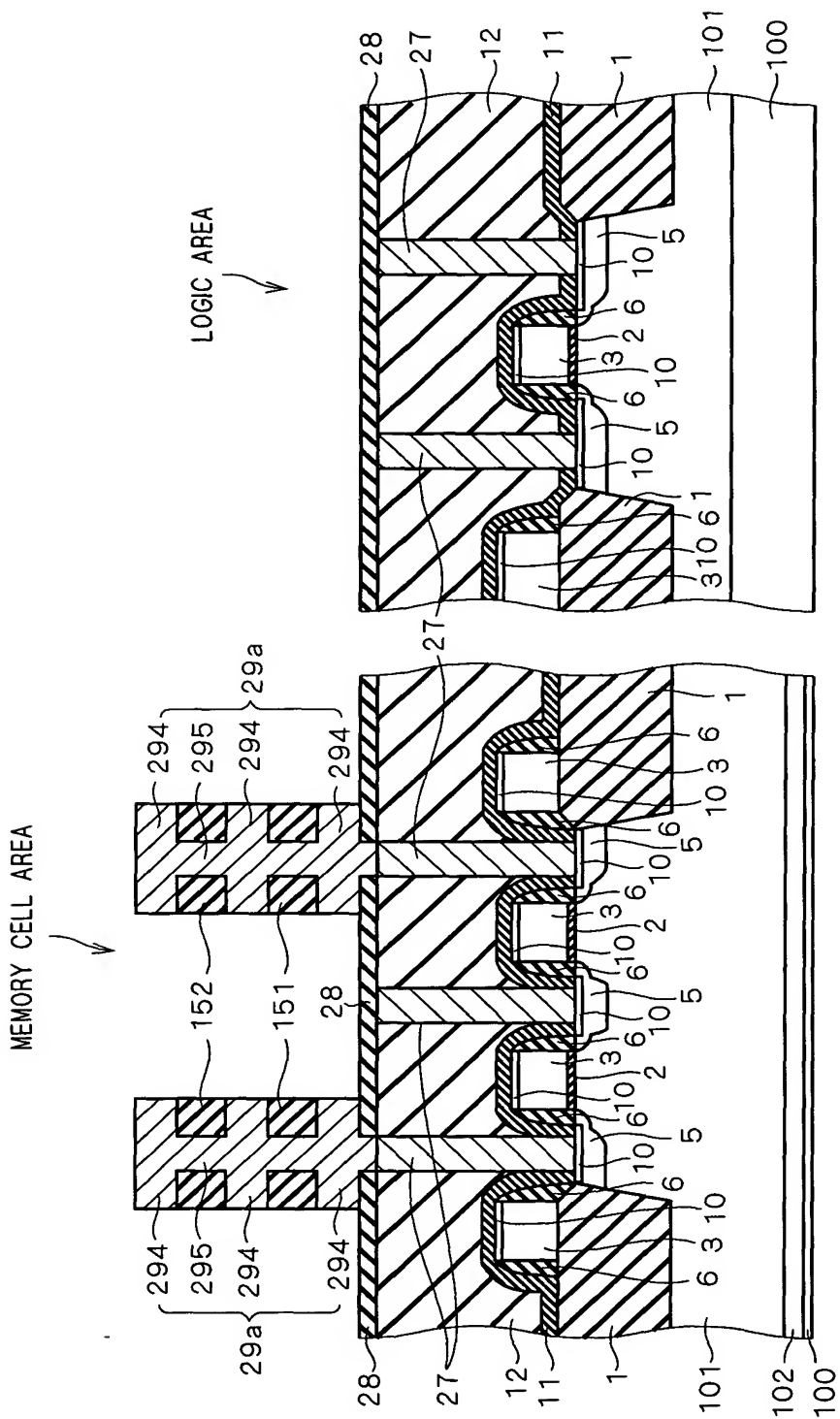
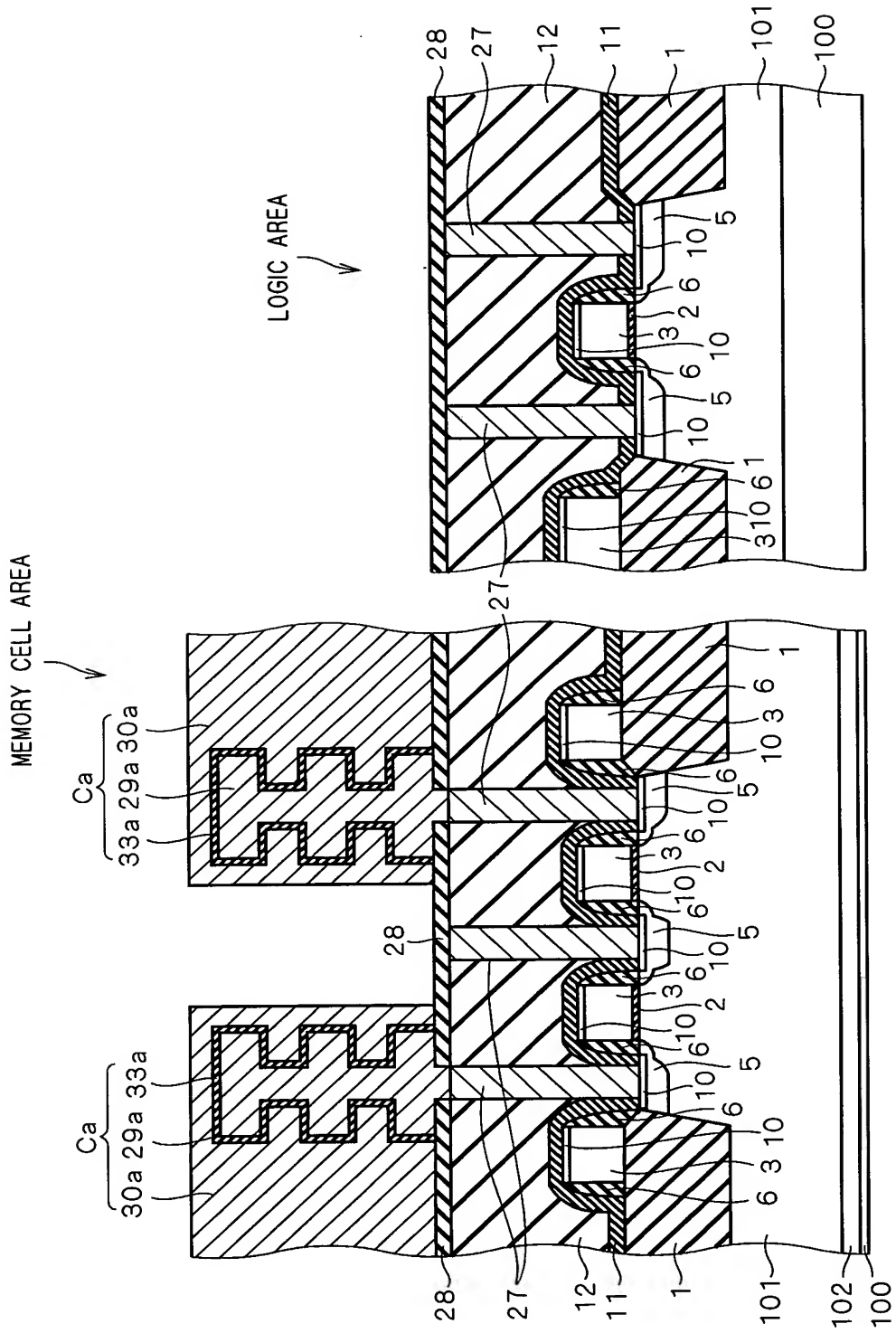


FIG. 11



F I G . 1 2

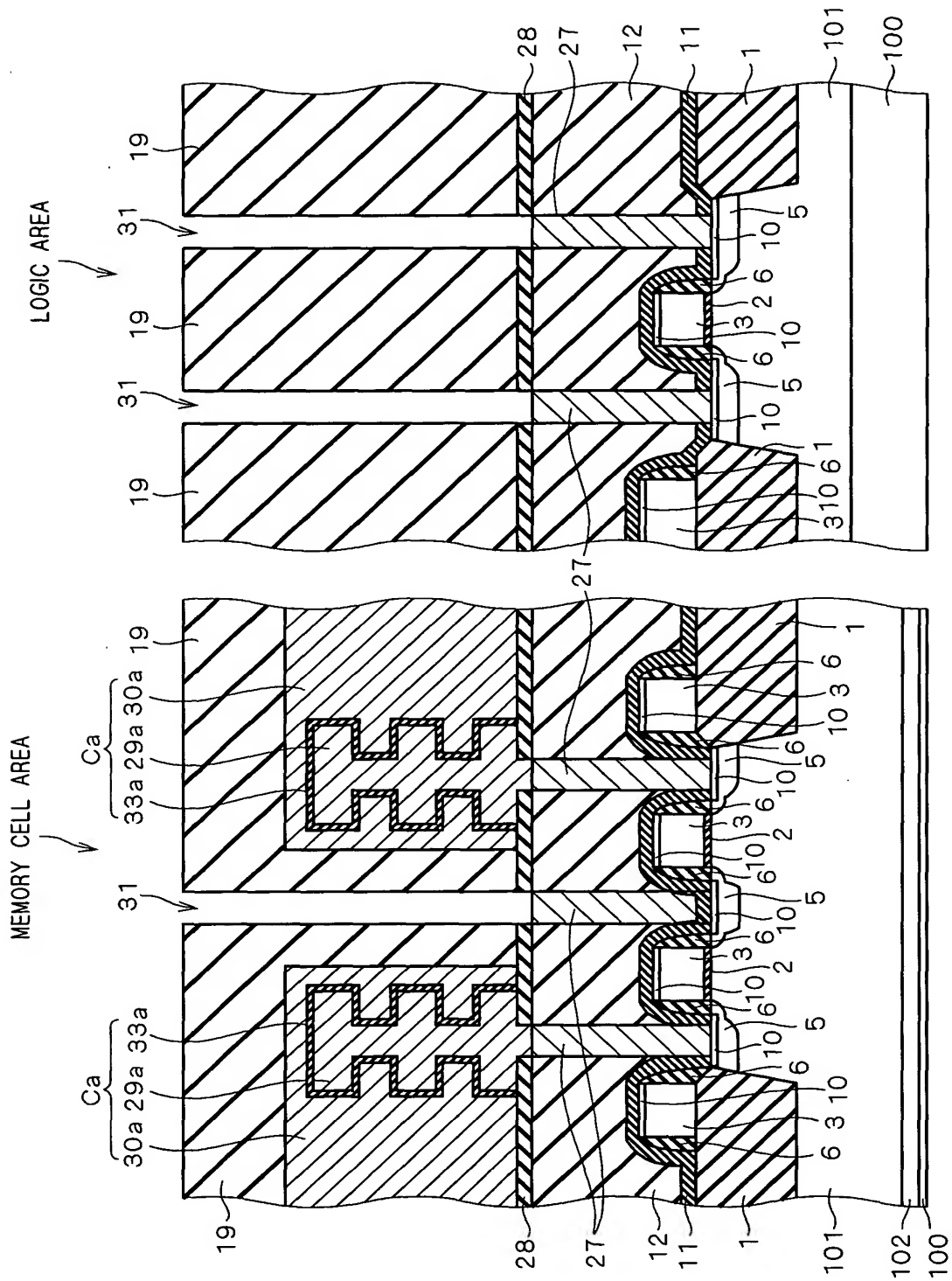


FIG. 13

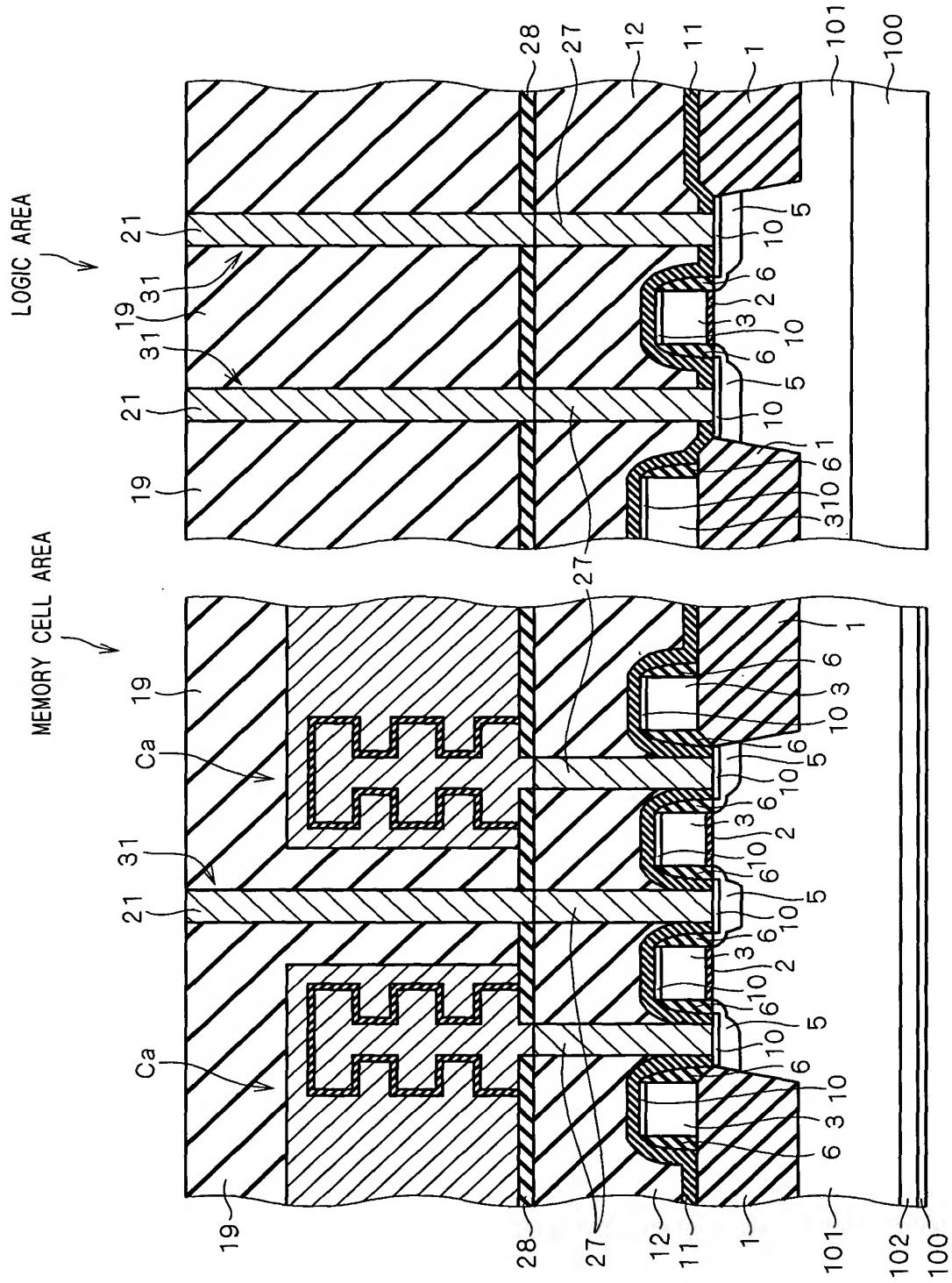


FIG. 14

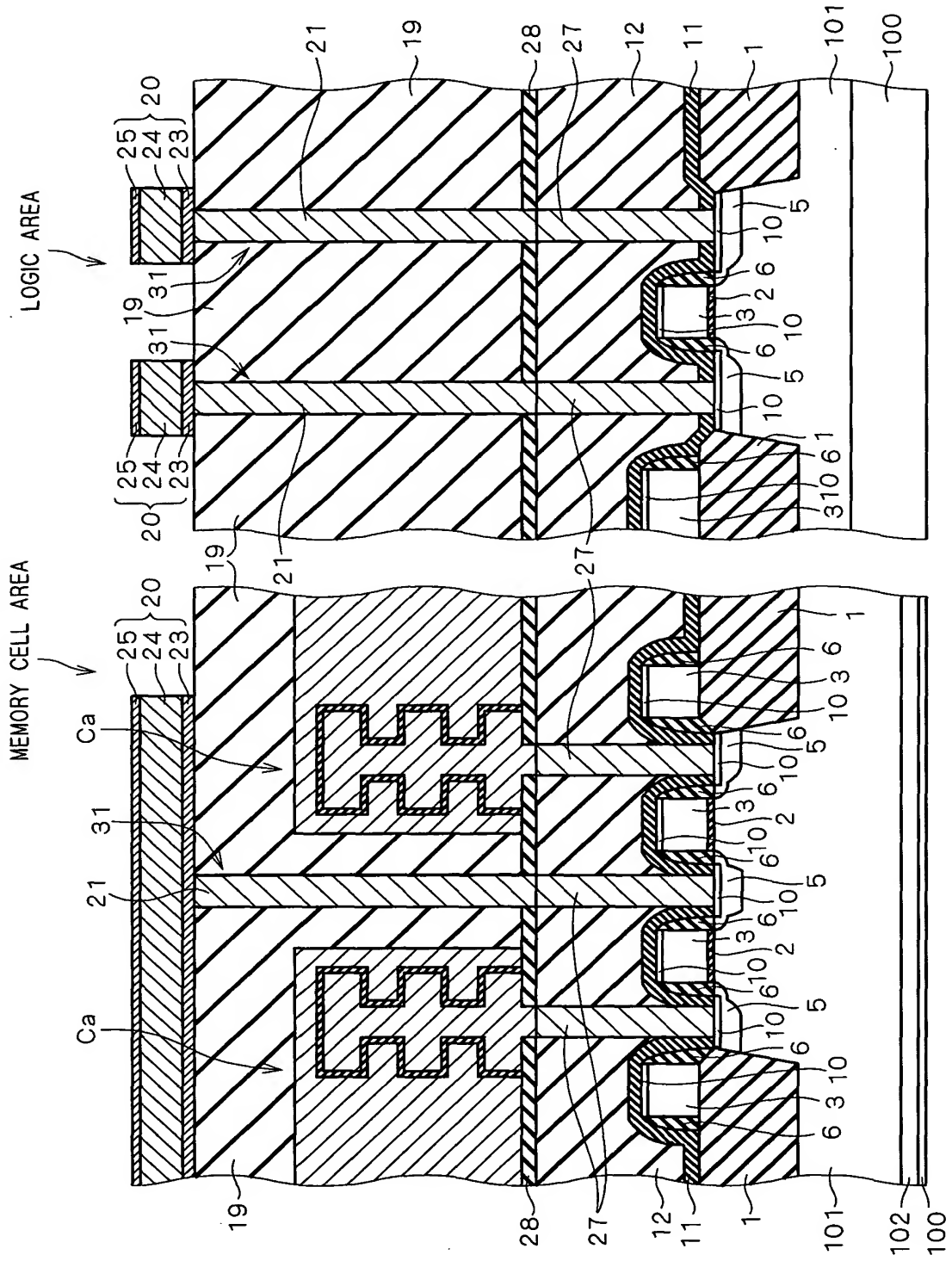


FIG. 15

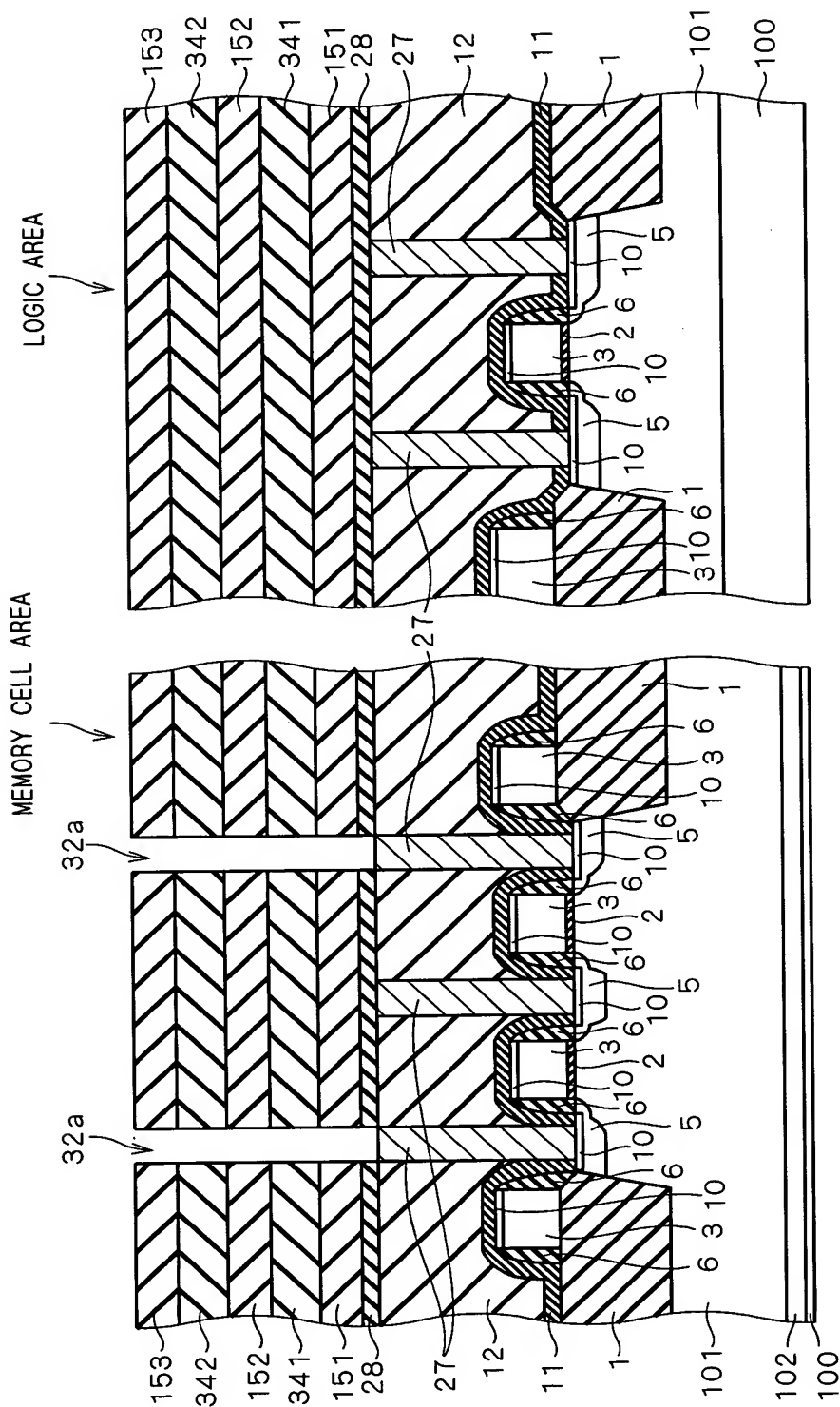


FIG. 16

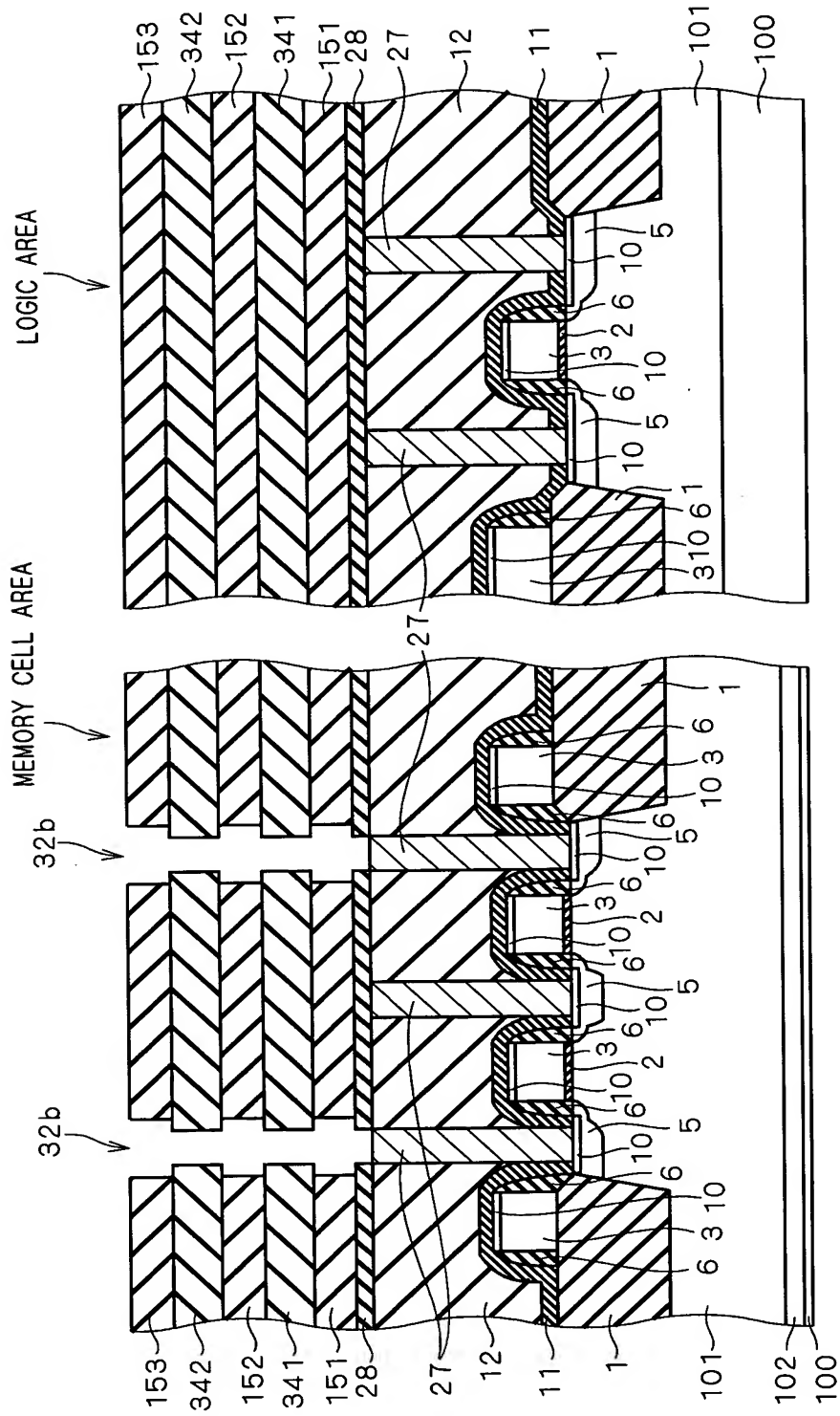
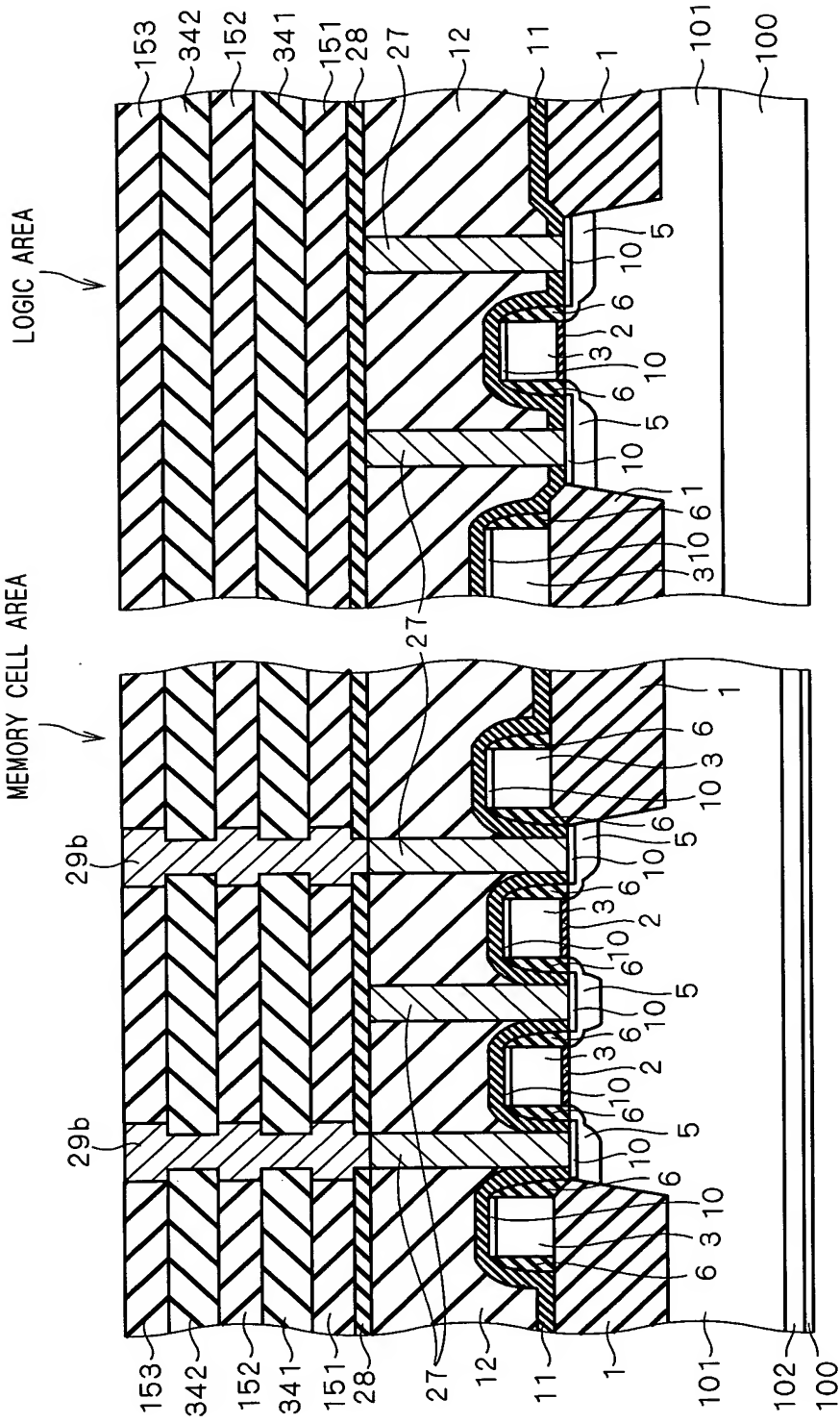


FIG. 17



F I G . 1 8

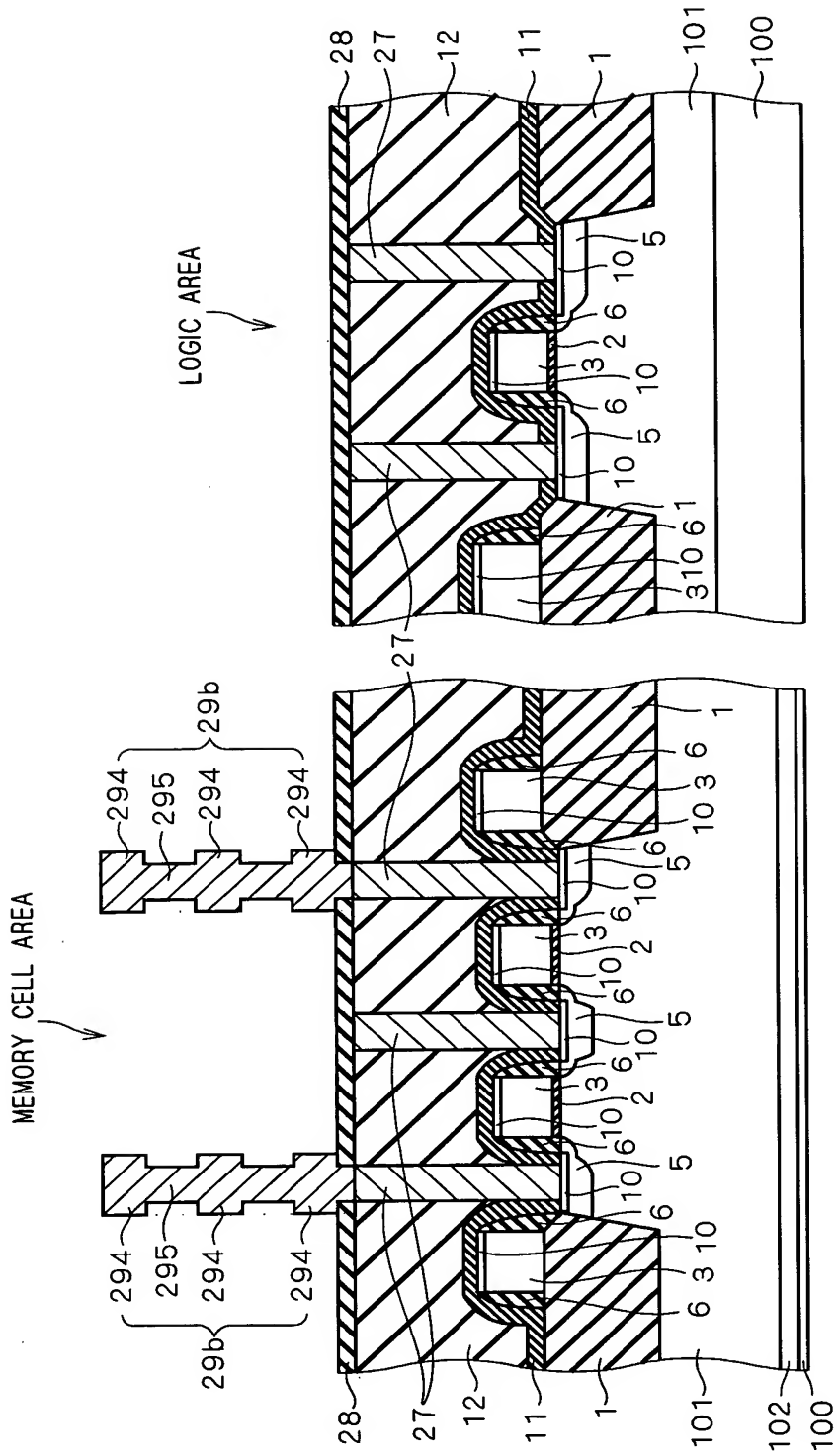


FIG. 19

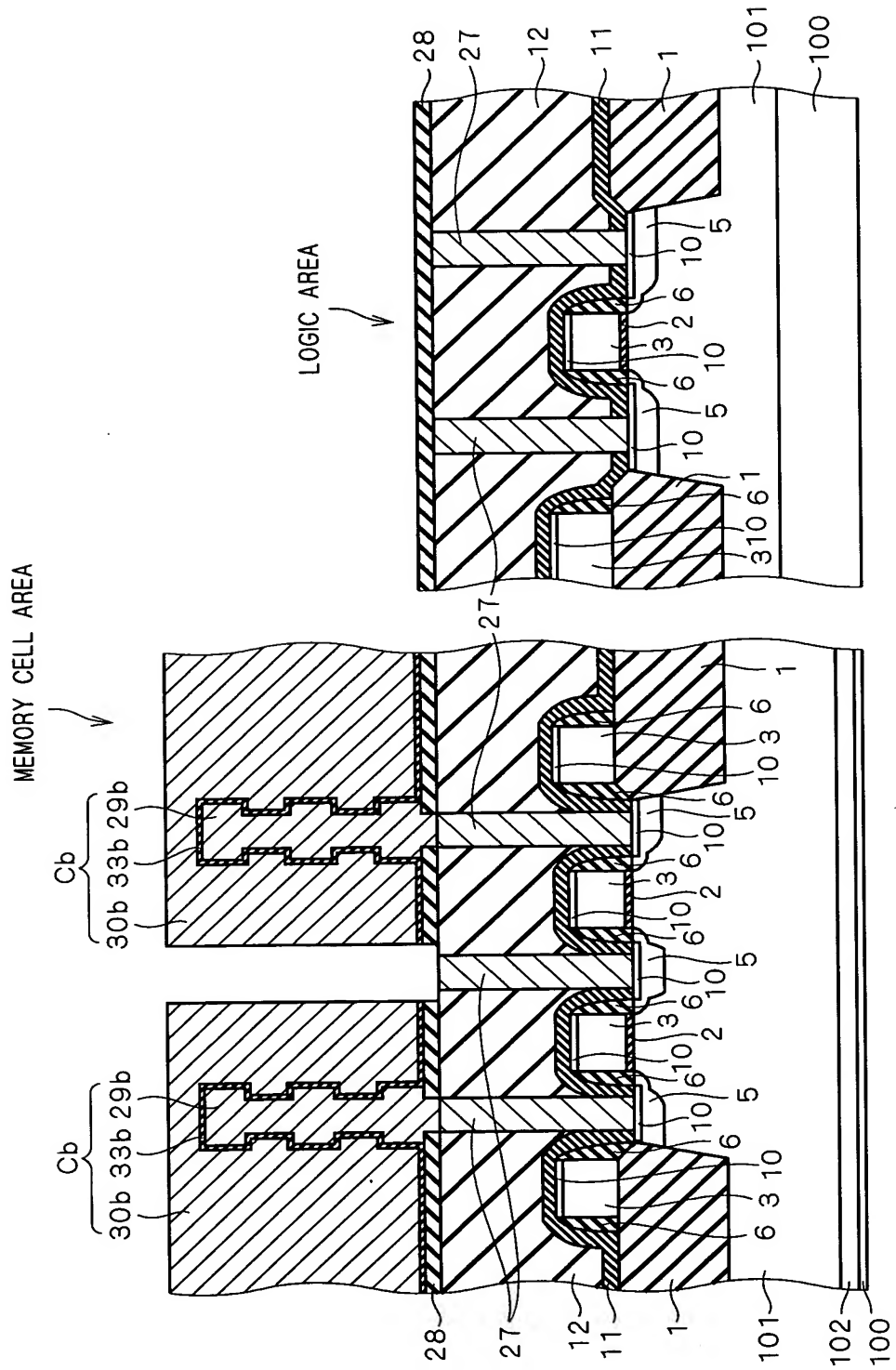
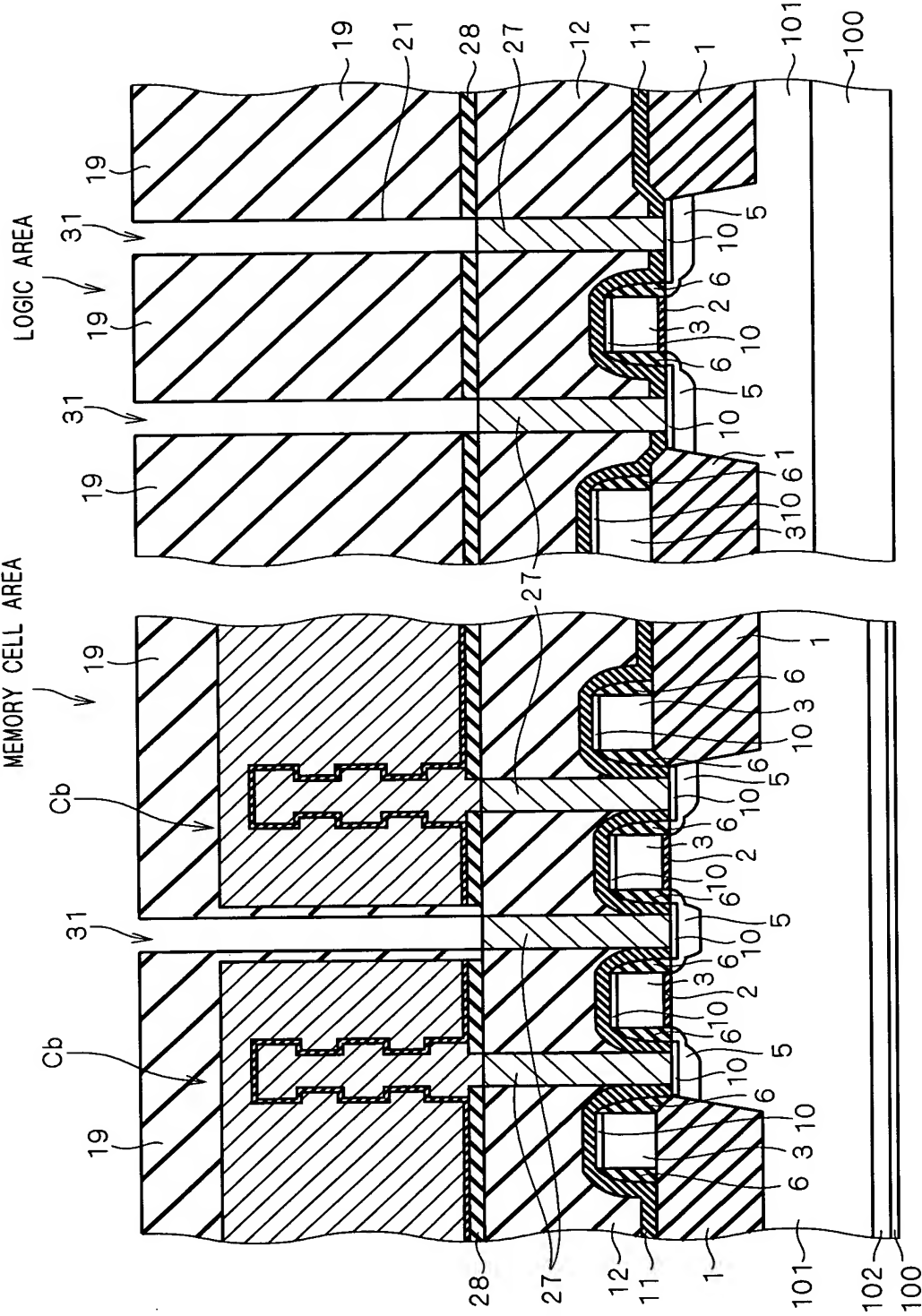
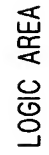
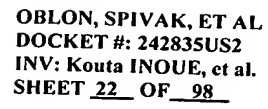


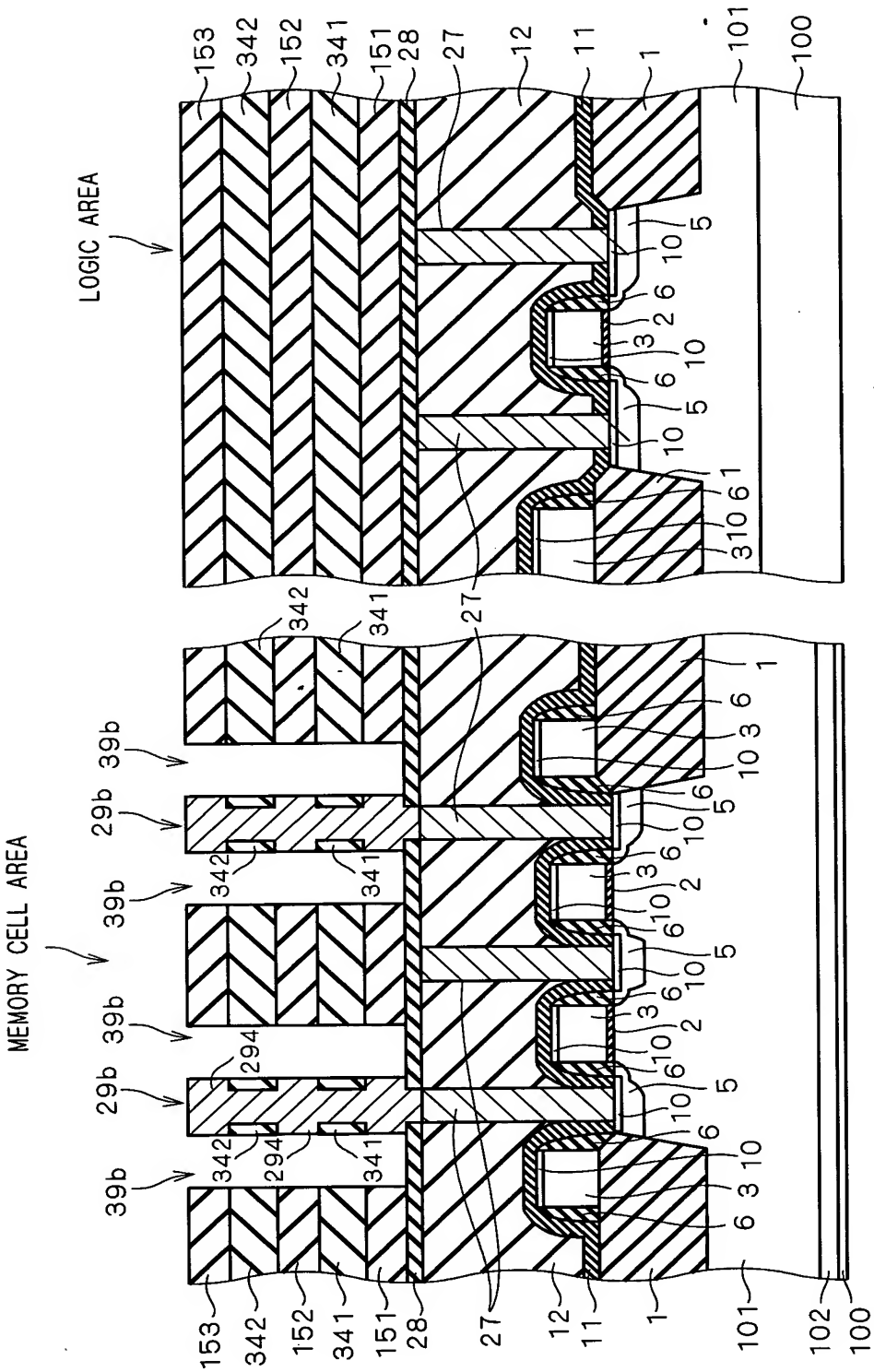
FIG. 20

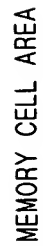




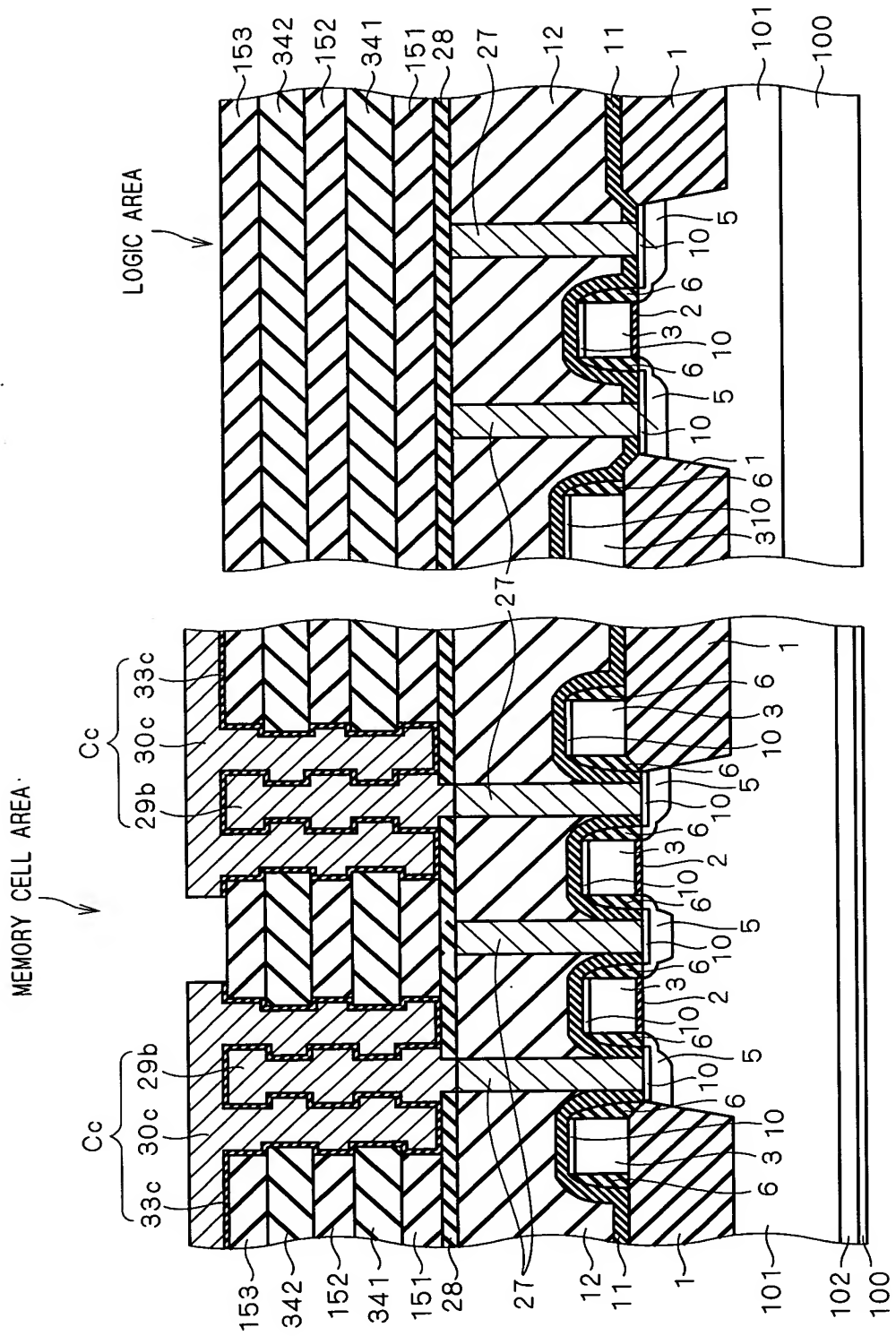


F I G . 2 3





F I G . 2 5



F I G . 2 6

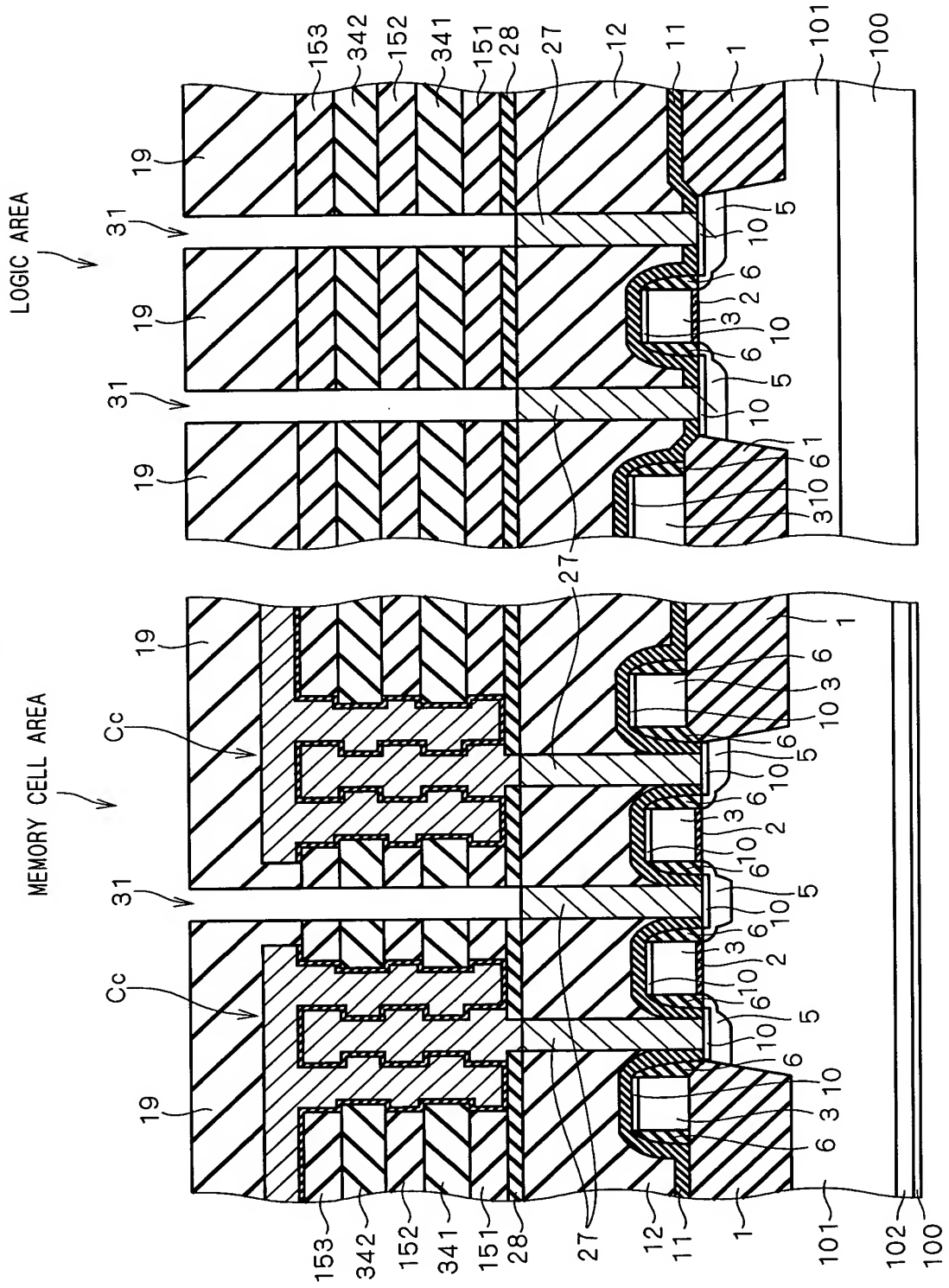


FIG. 27

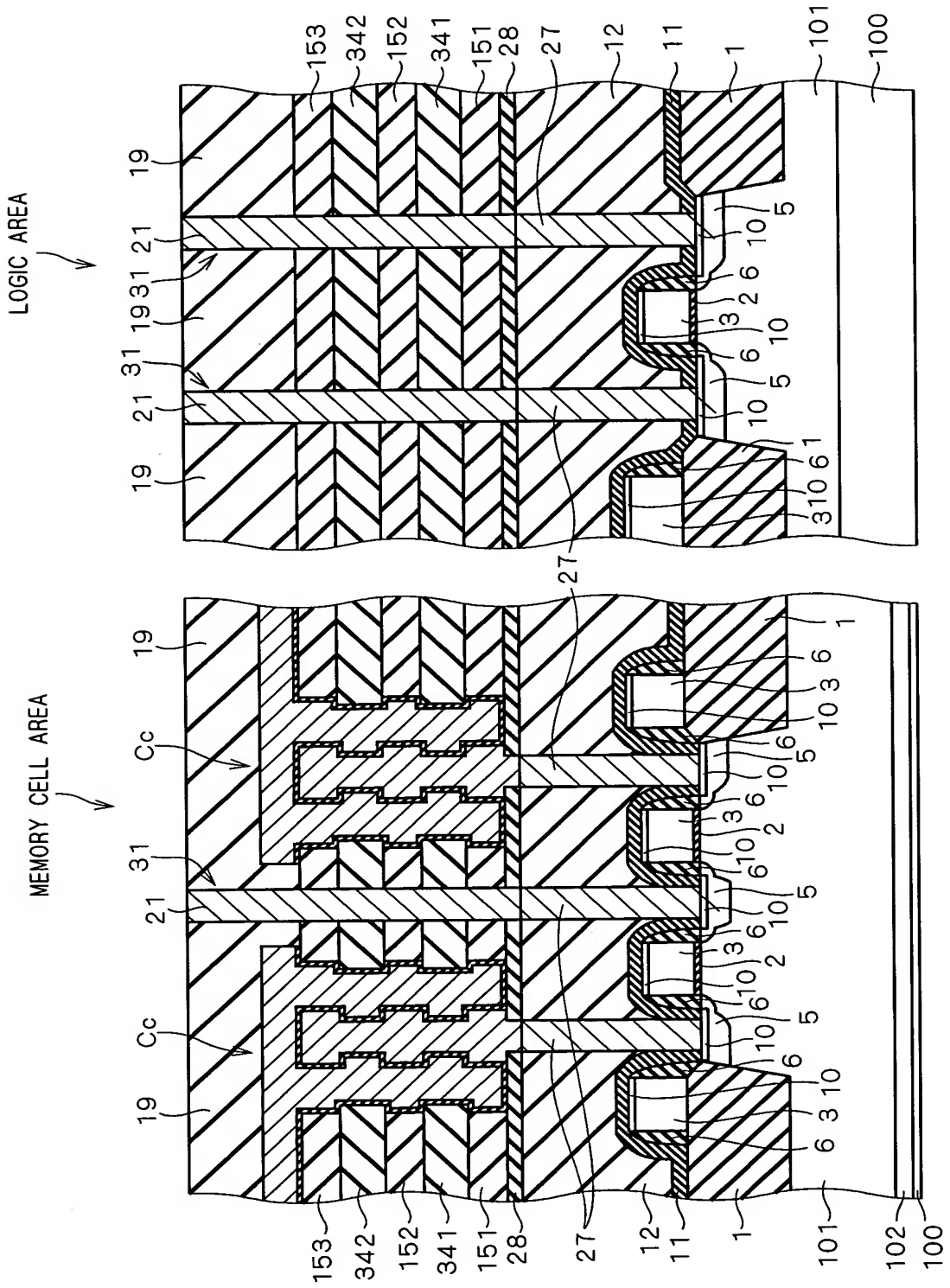


FIG. 28

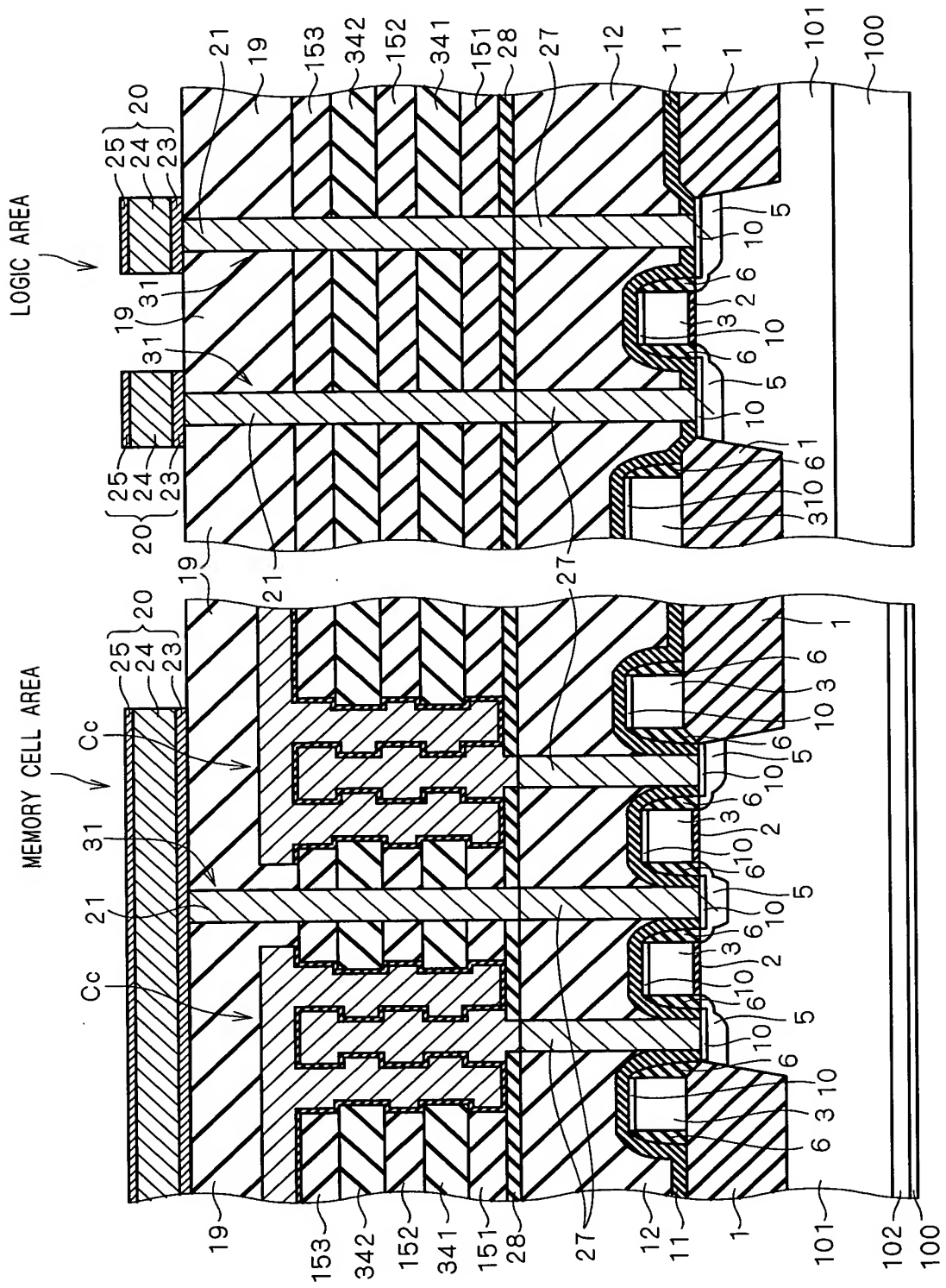


FIG. 29

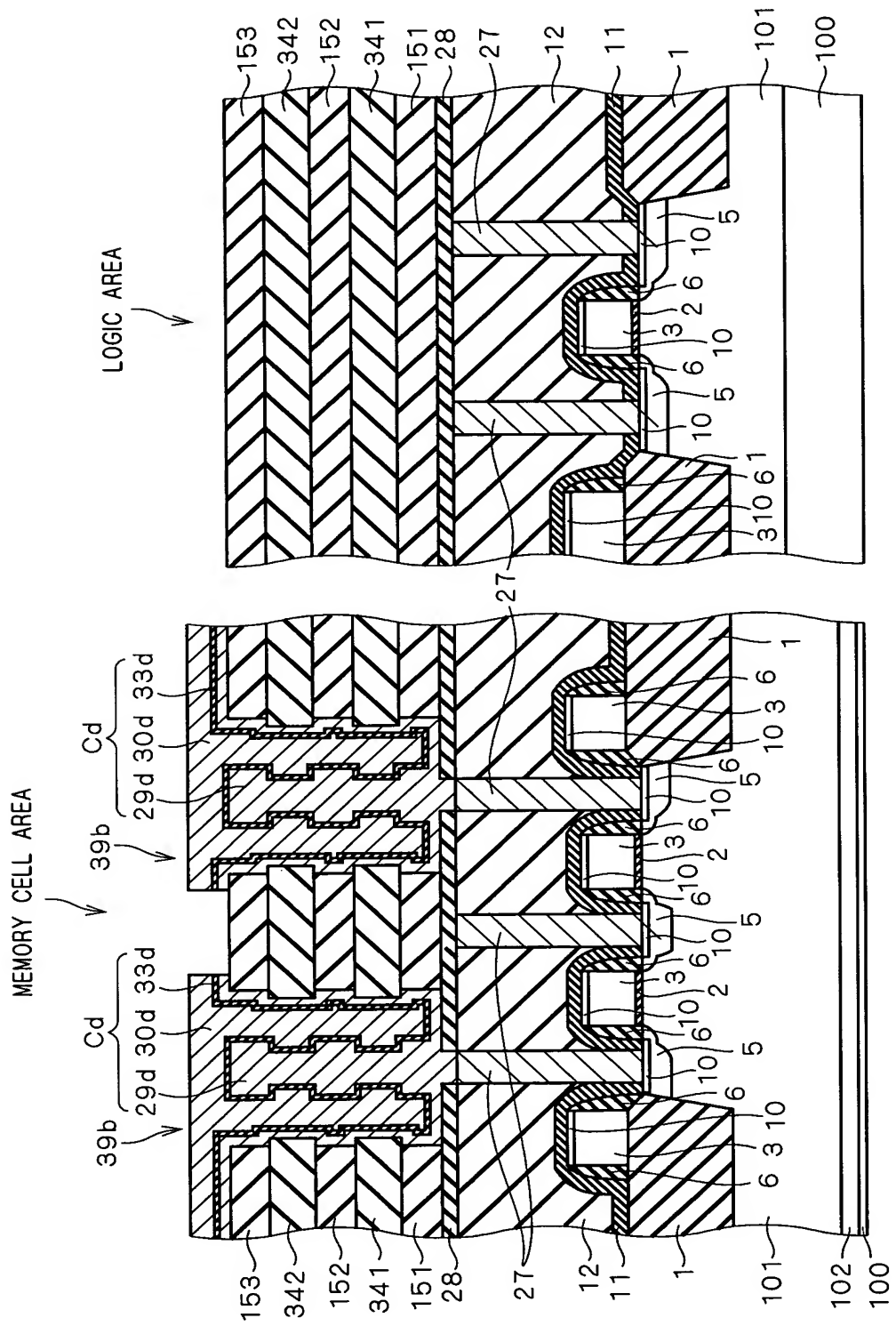
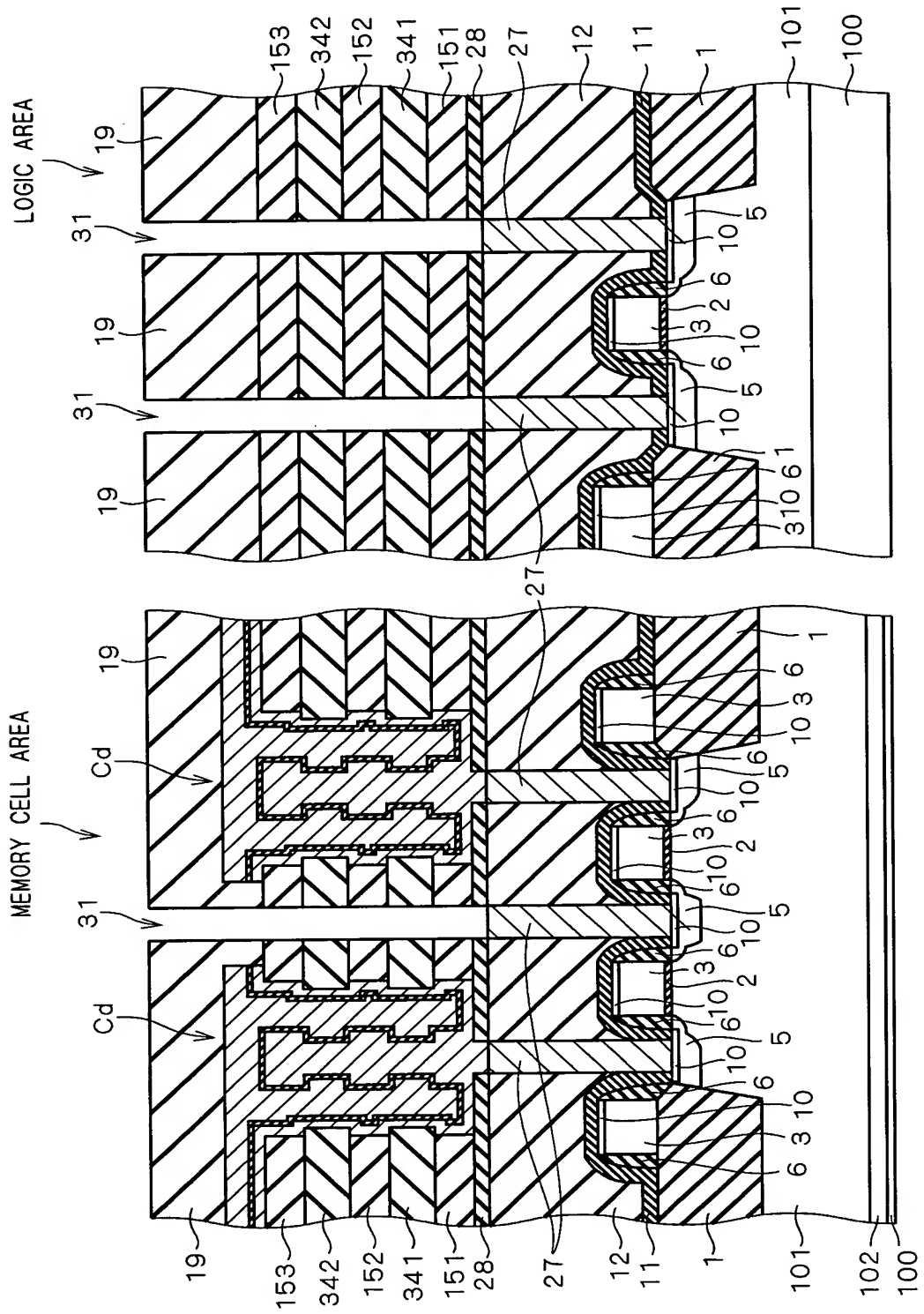
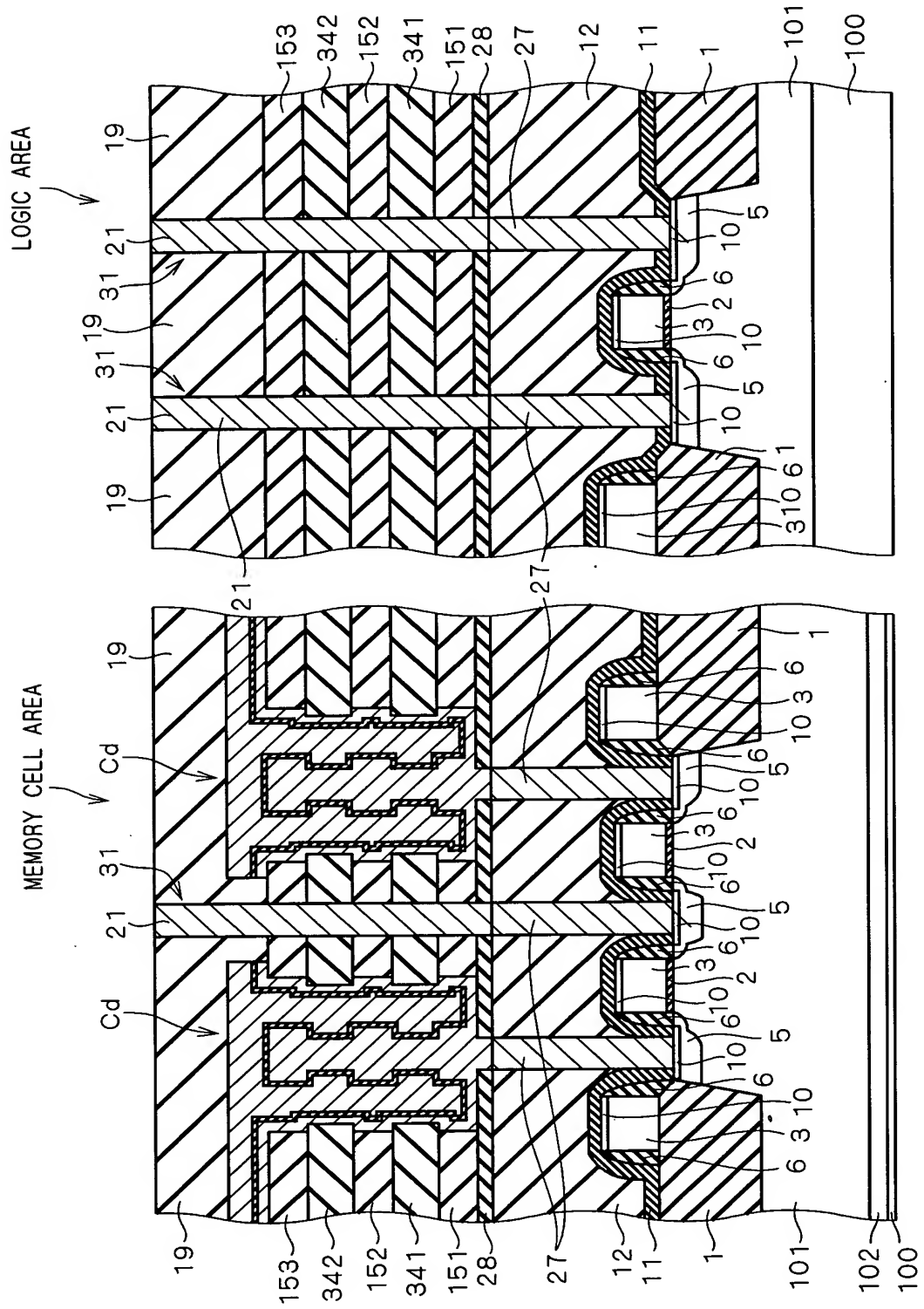


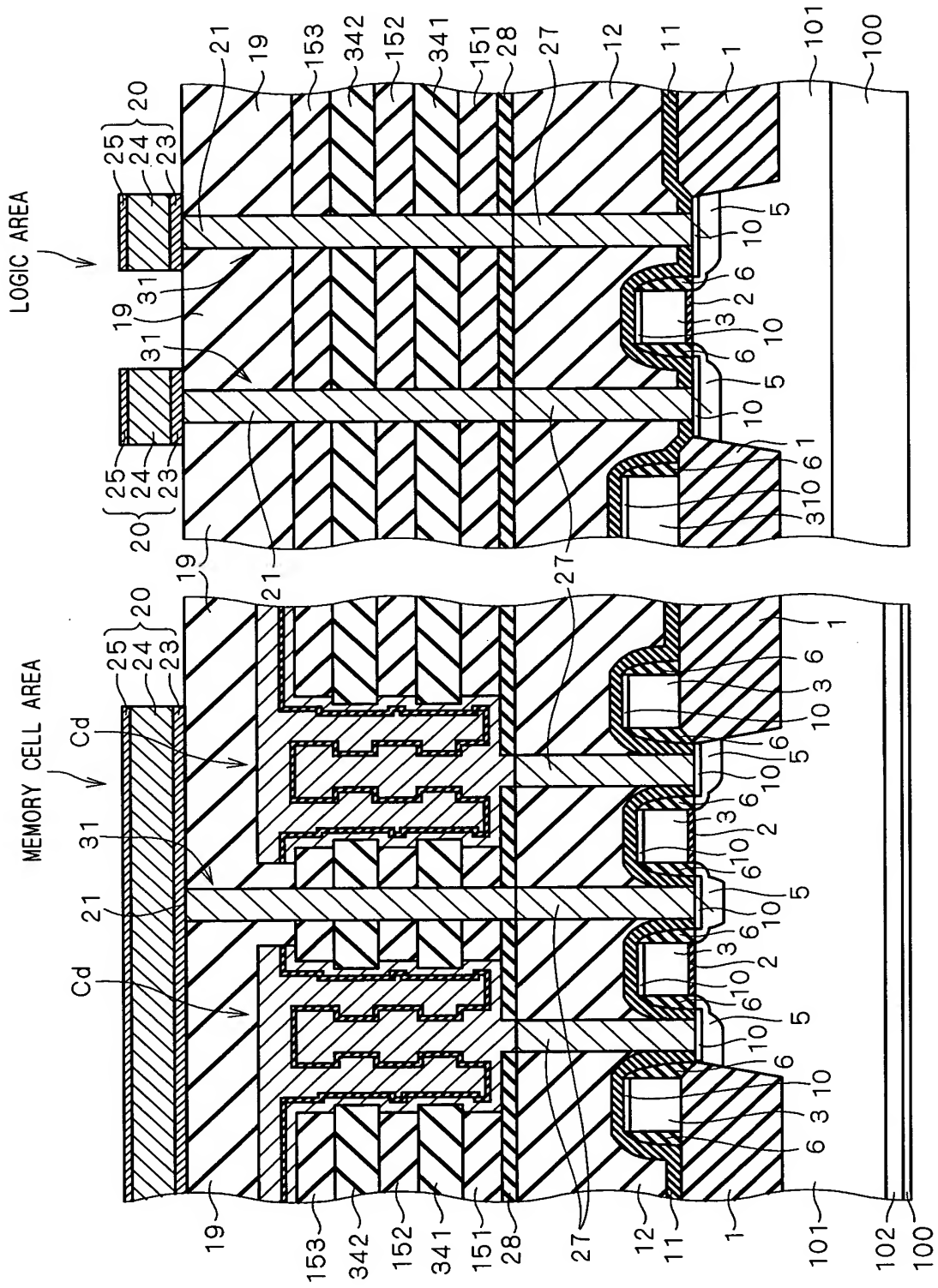
FIG. 30



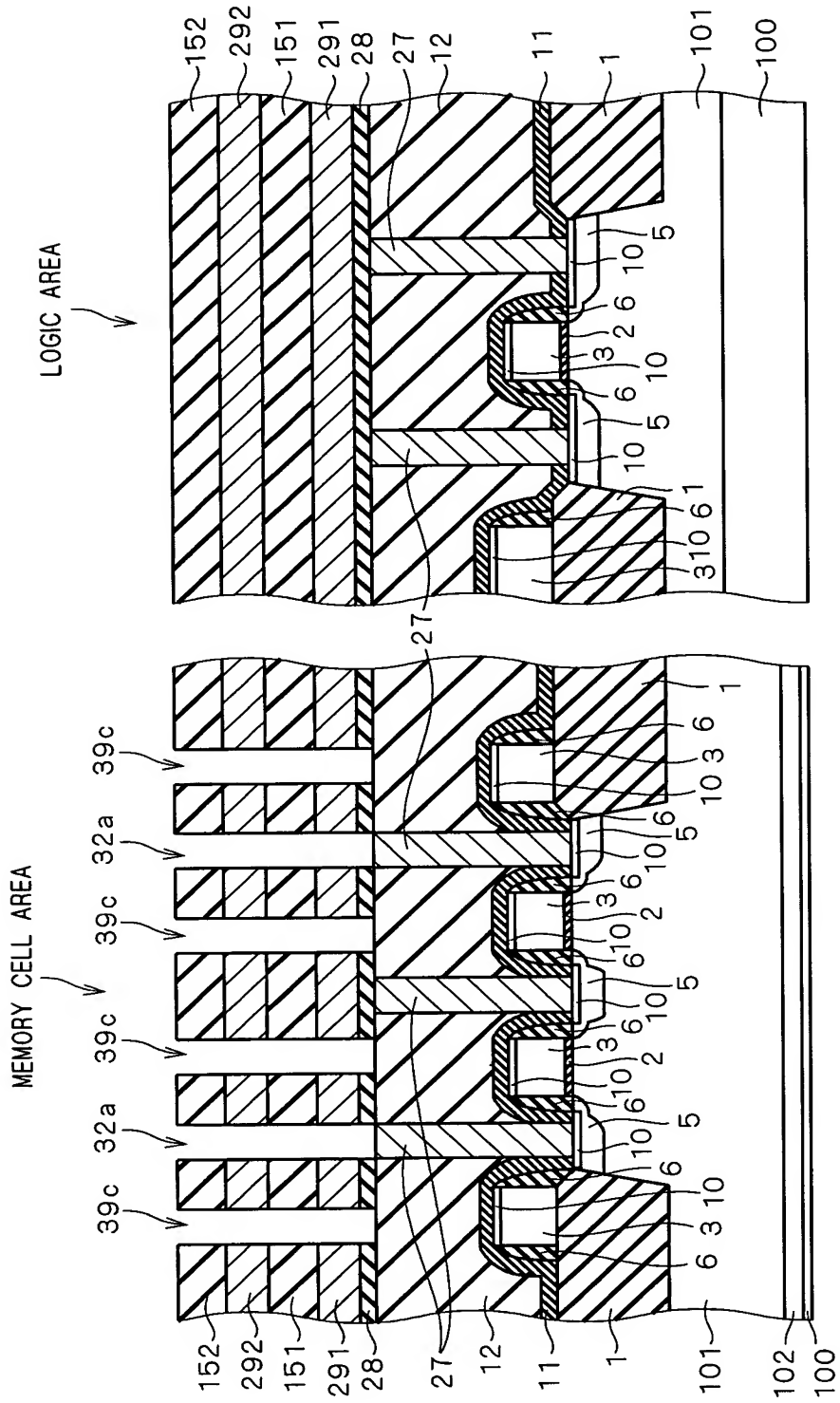
F I G . 3 1



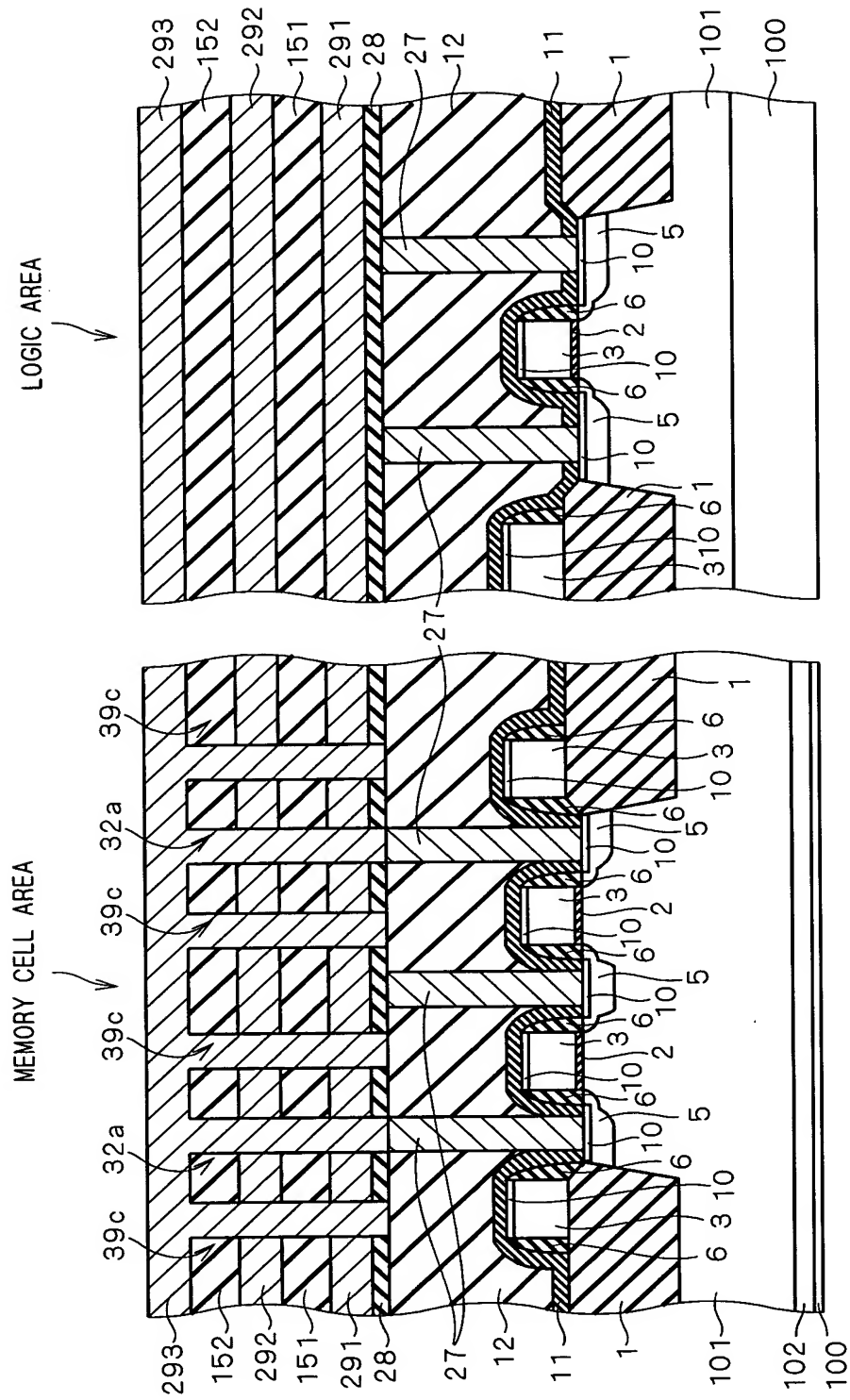
F I G . 3 2

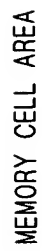


F I G . 3 3



F I G . 3 4





F I G . 3 6

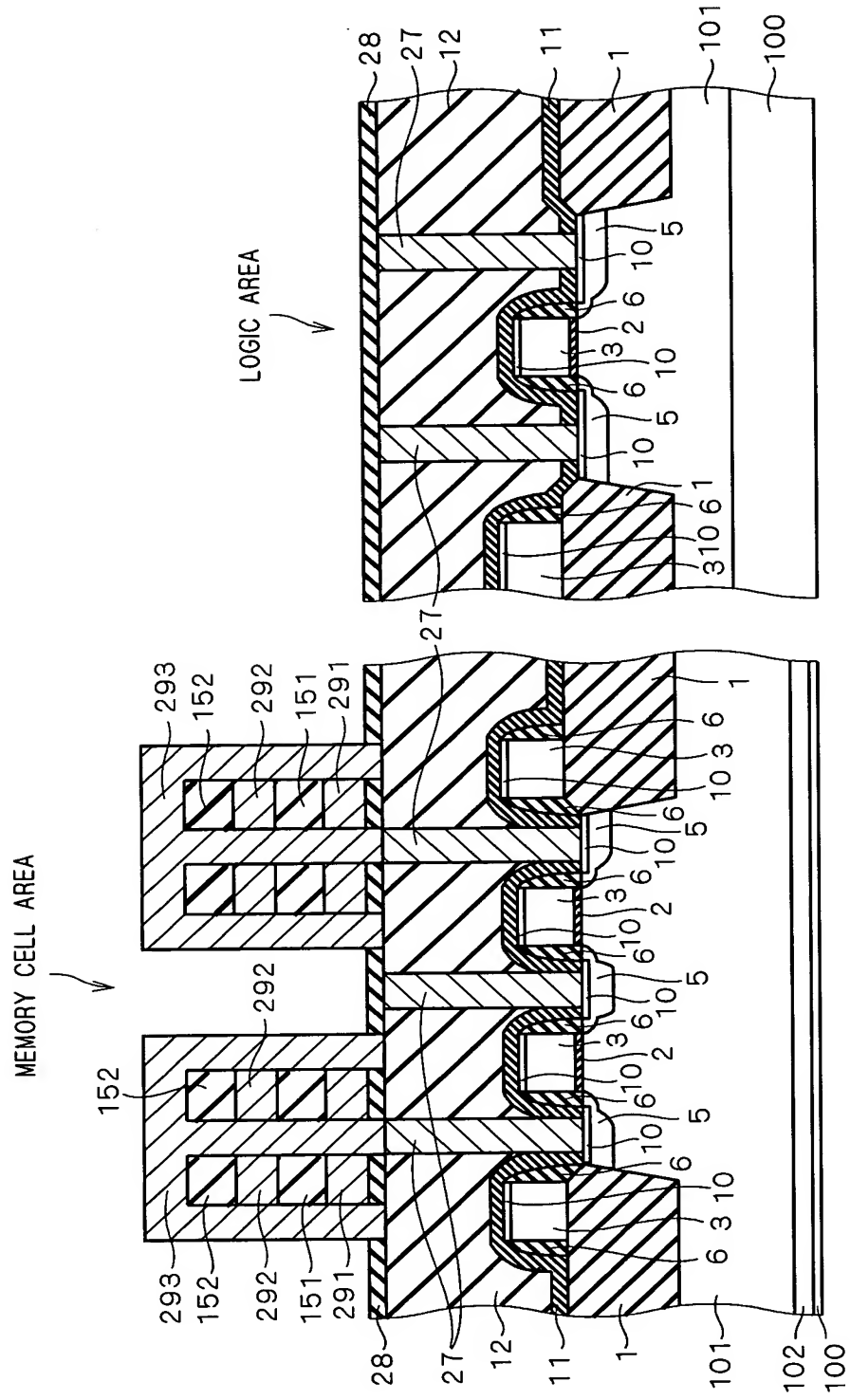
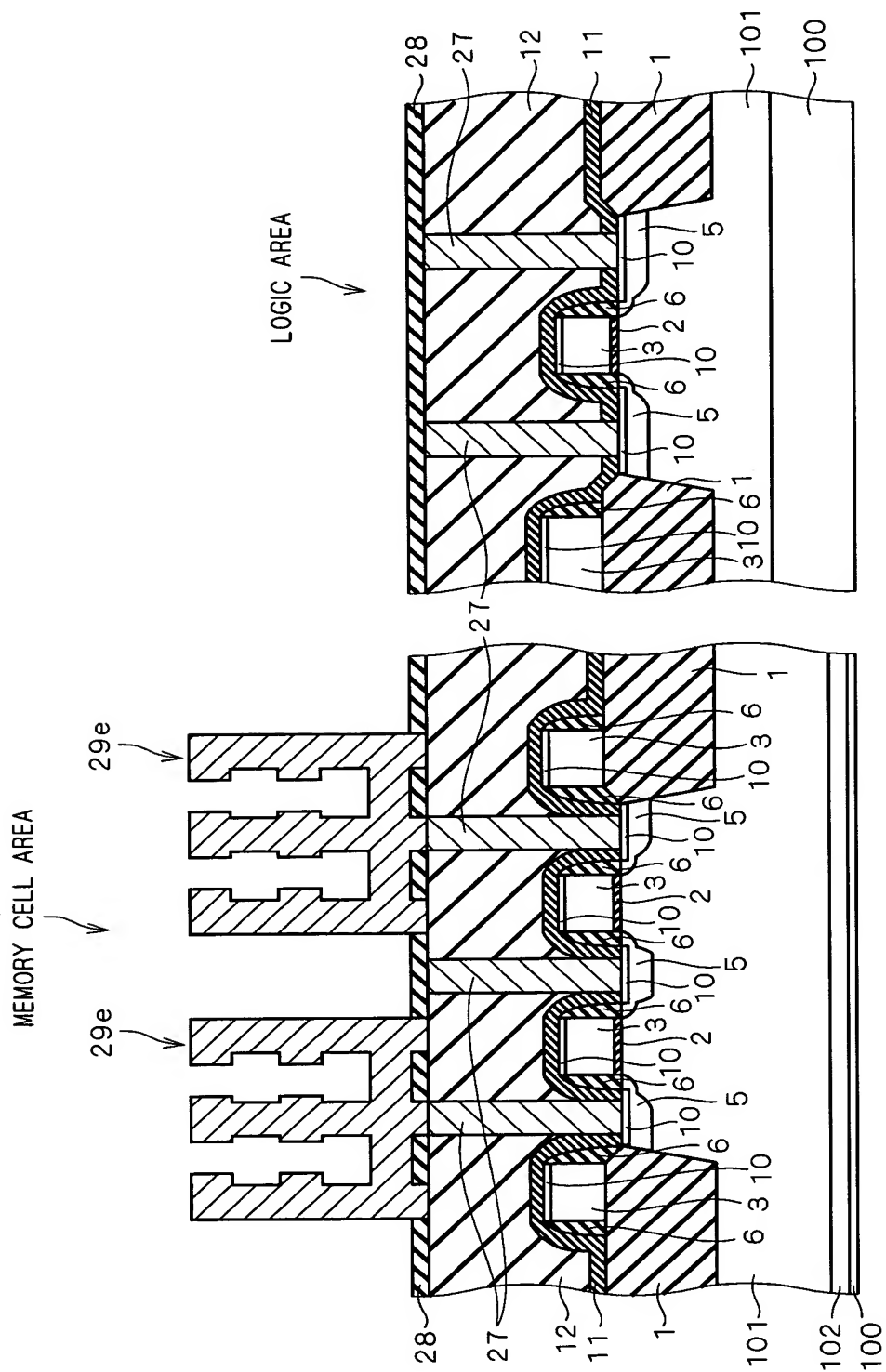


FIG. 37

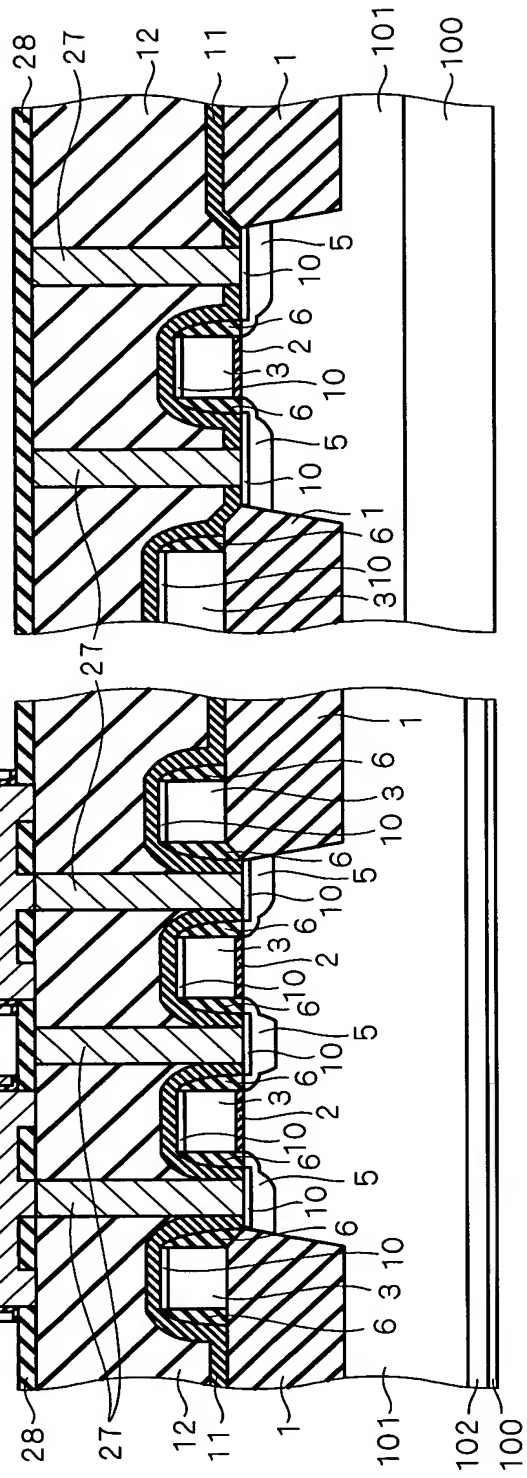


F I G . 3 8

MEMORY CELL AREA

Ce  
29e 33e 30e  
Ce  
29e 33e 30e

LOGIC AREA



F I G . 3 9

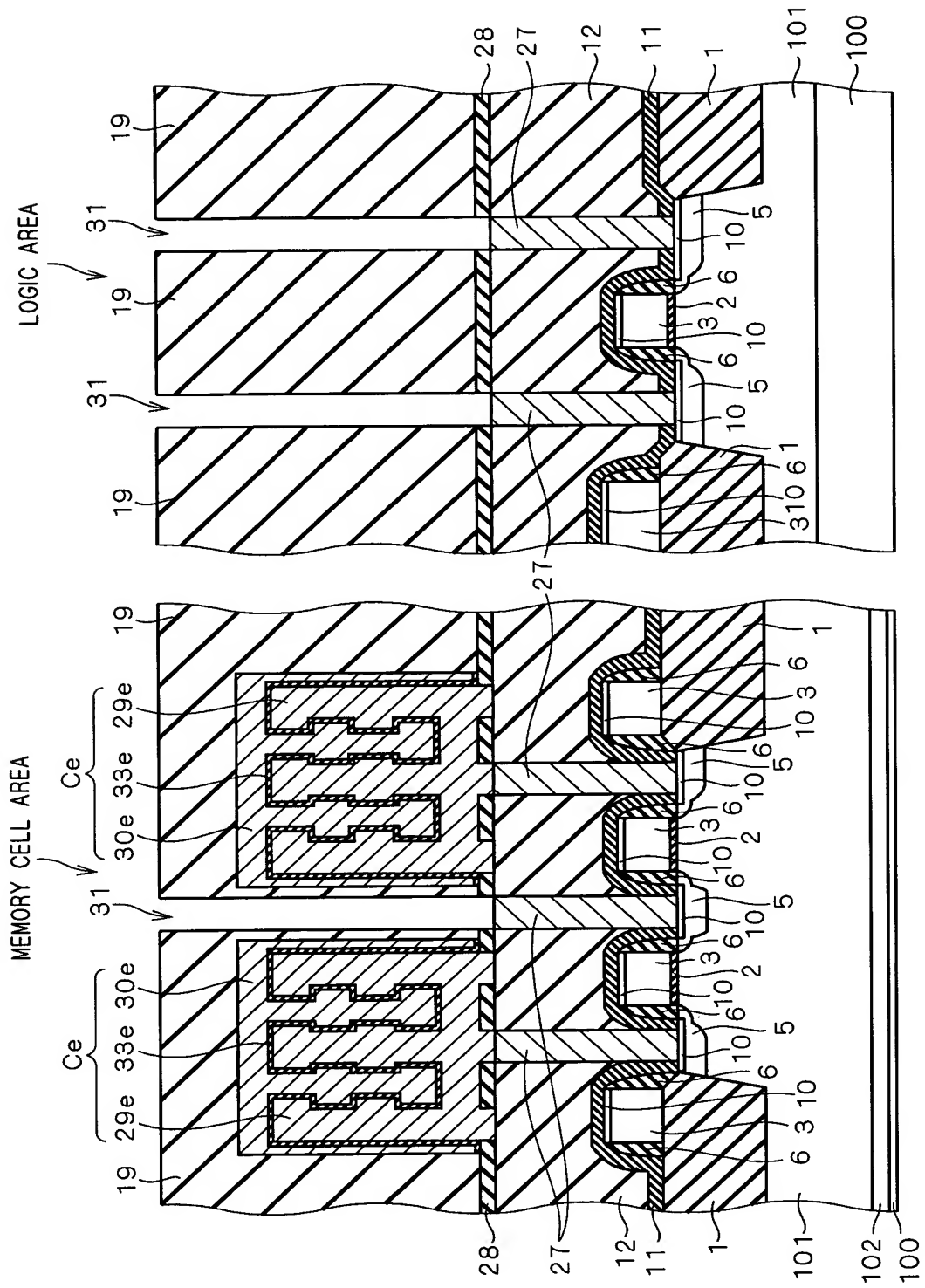
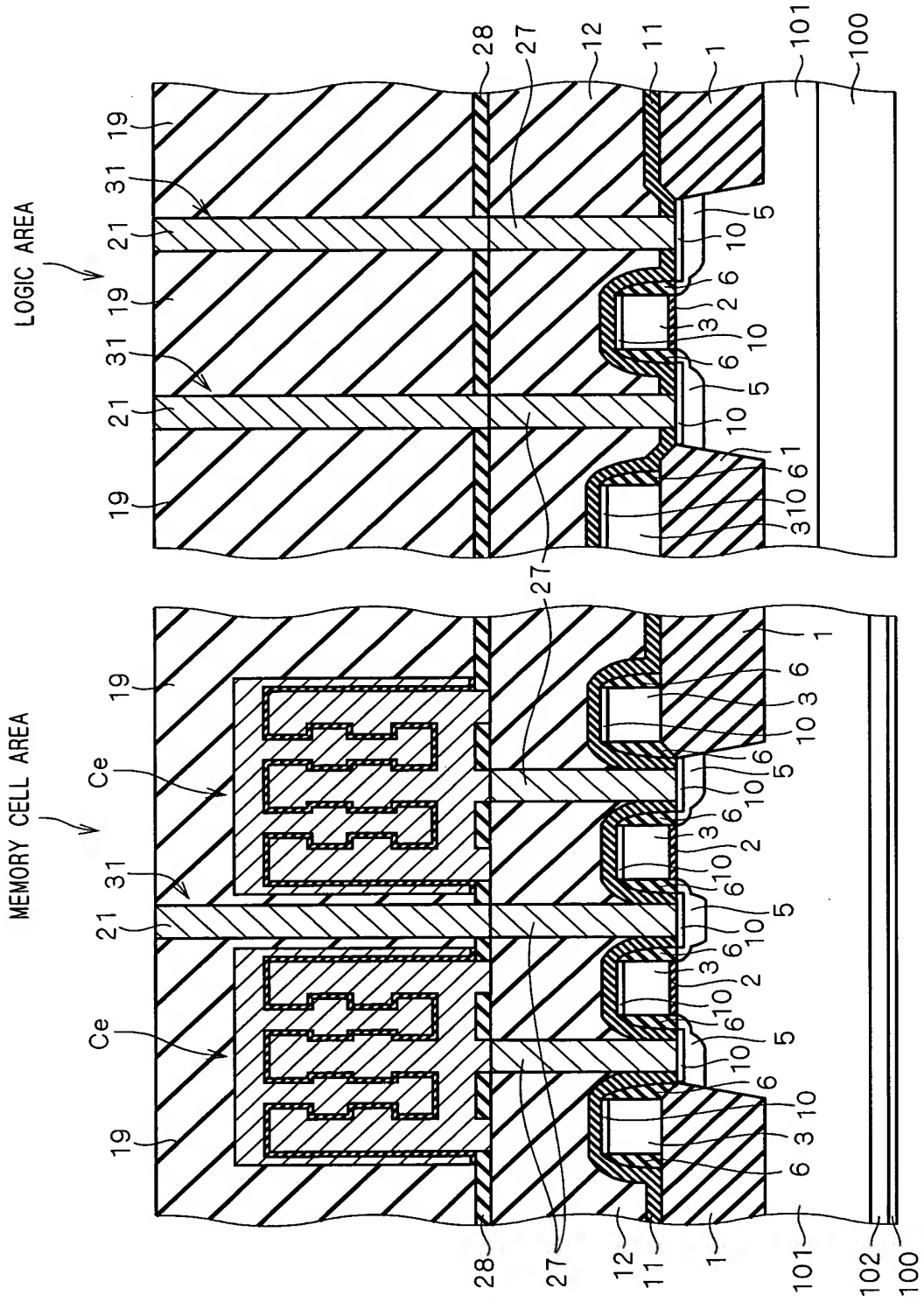
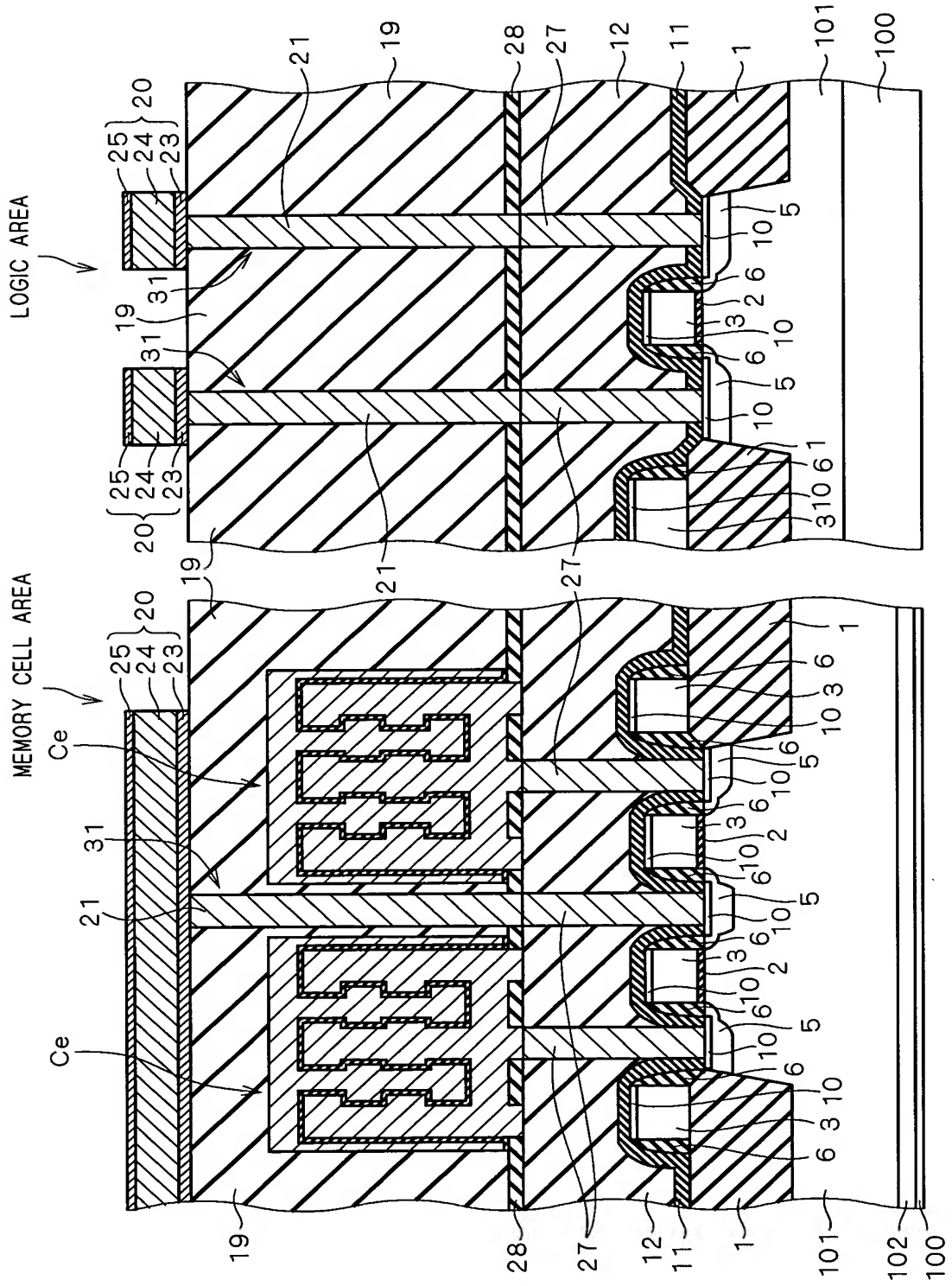


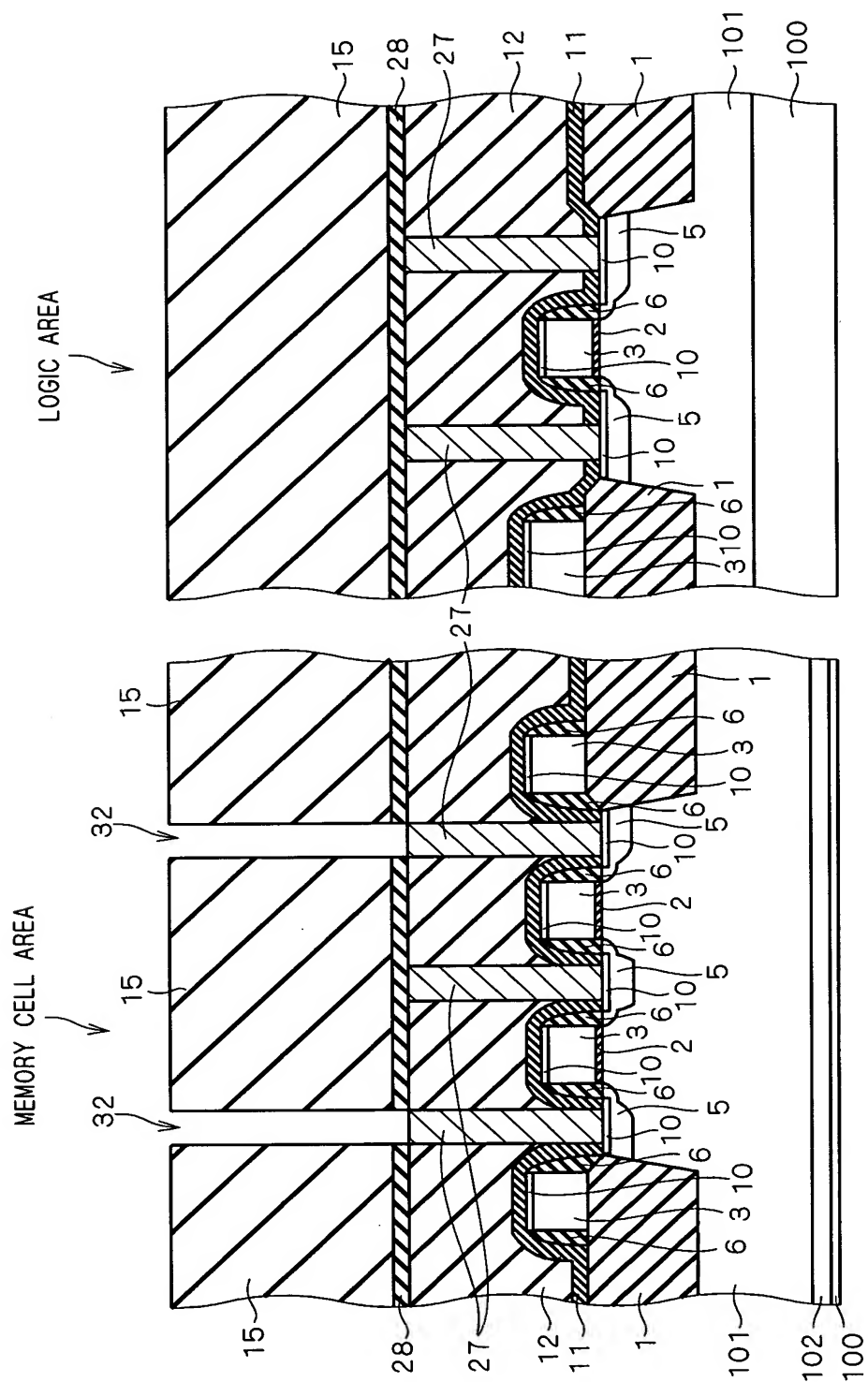
FIG. 40



F I G . 4 1



F I G . 4 2



F I G . 4 3

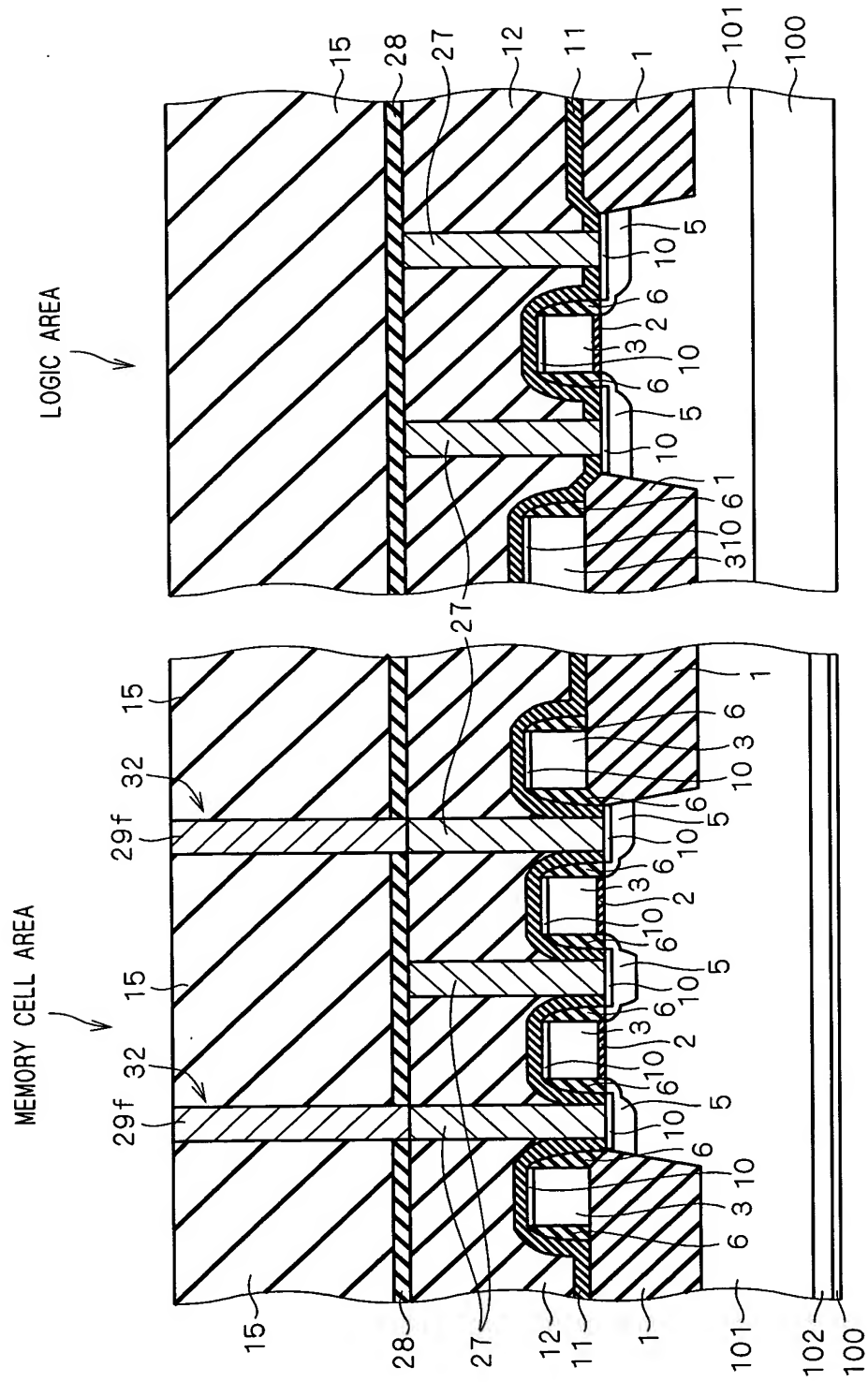
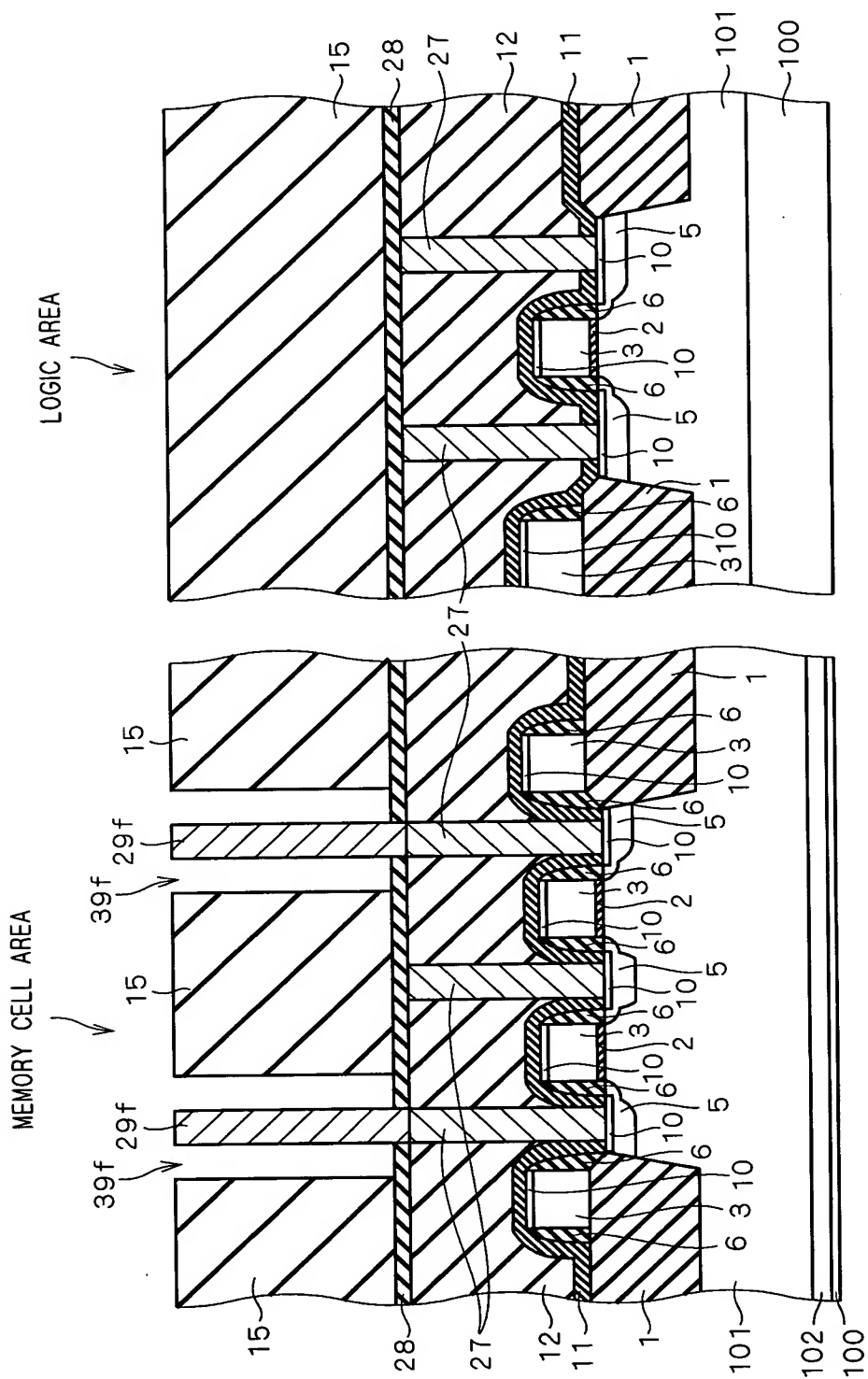
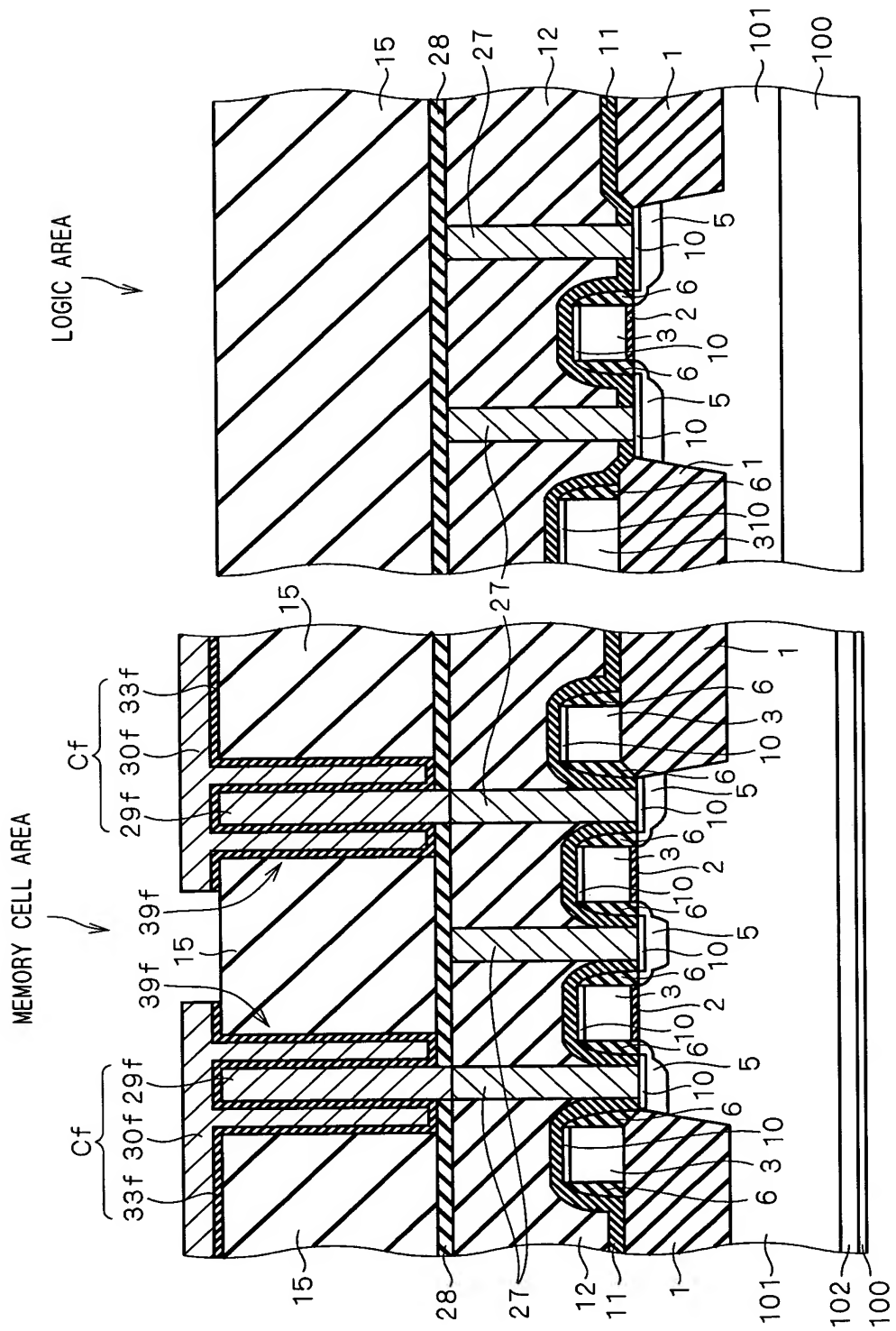


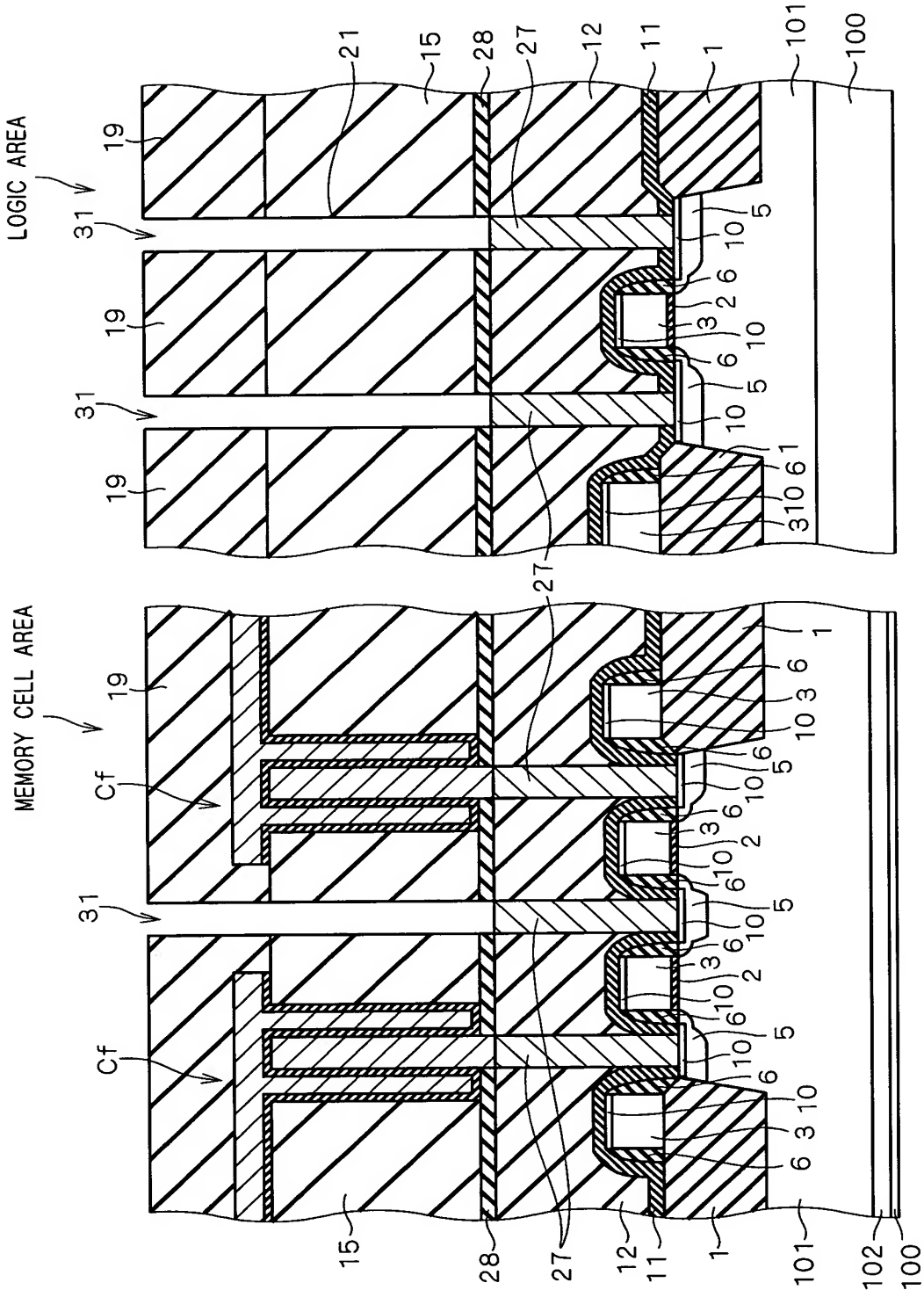
FIG. 44



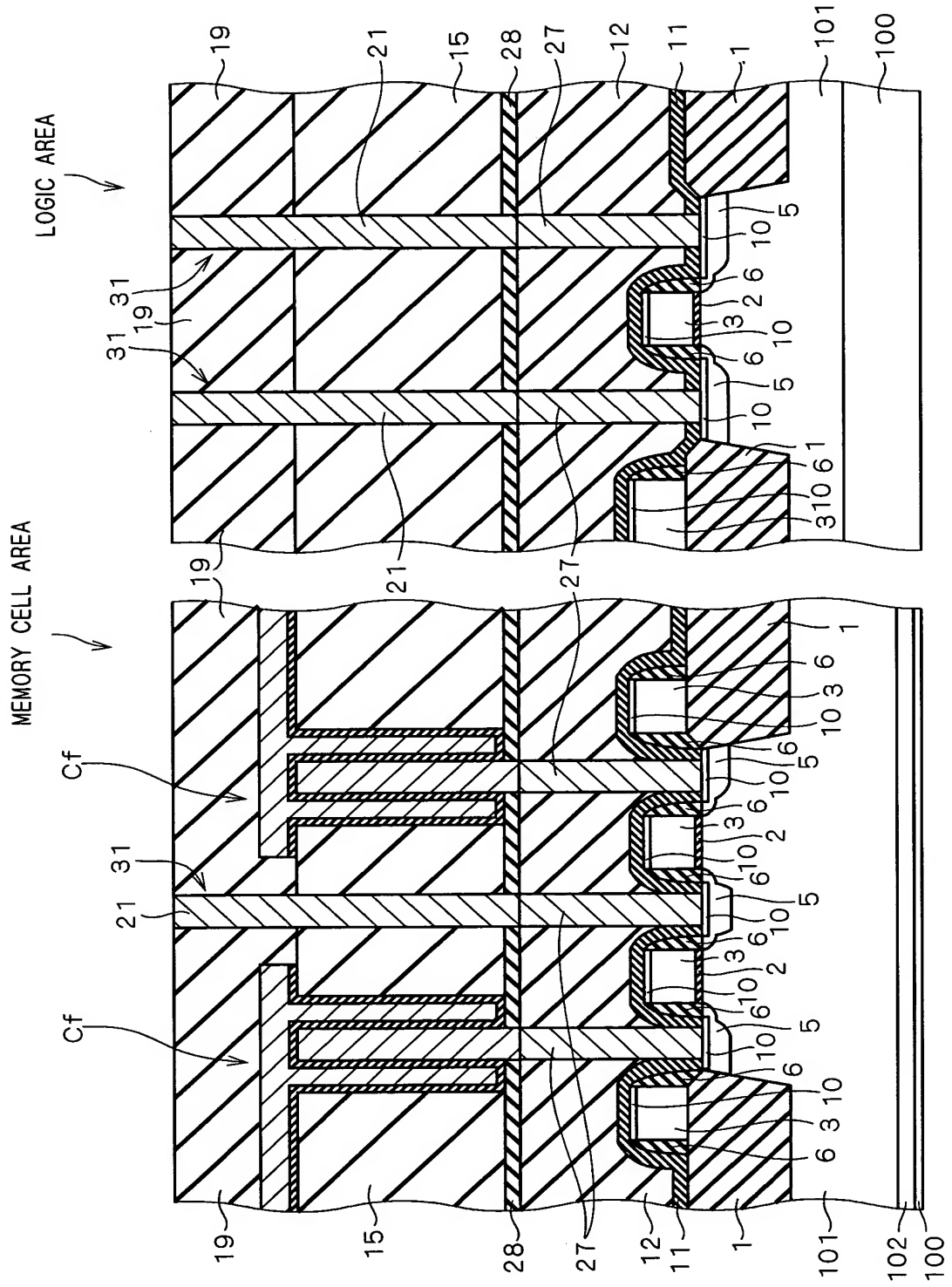
F I G . 4 5



F I G . 4 6



F I G . 4 7



F I G . 4 8

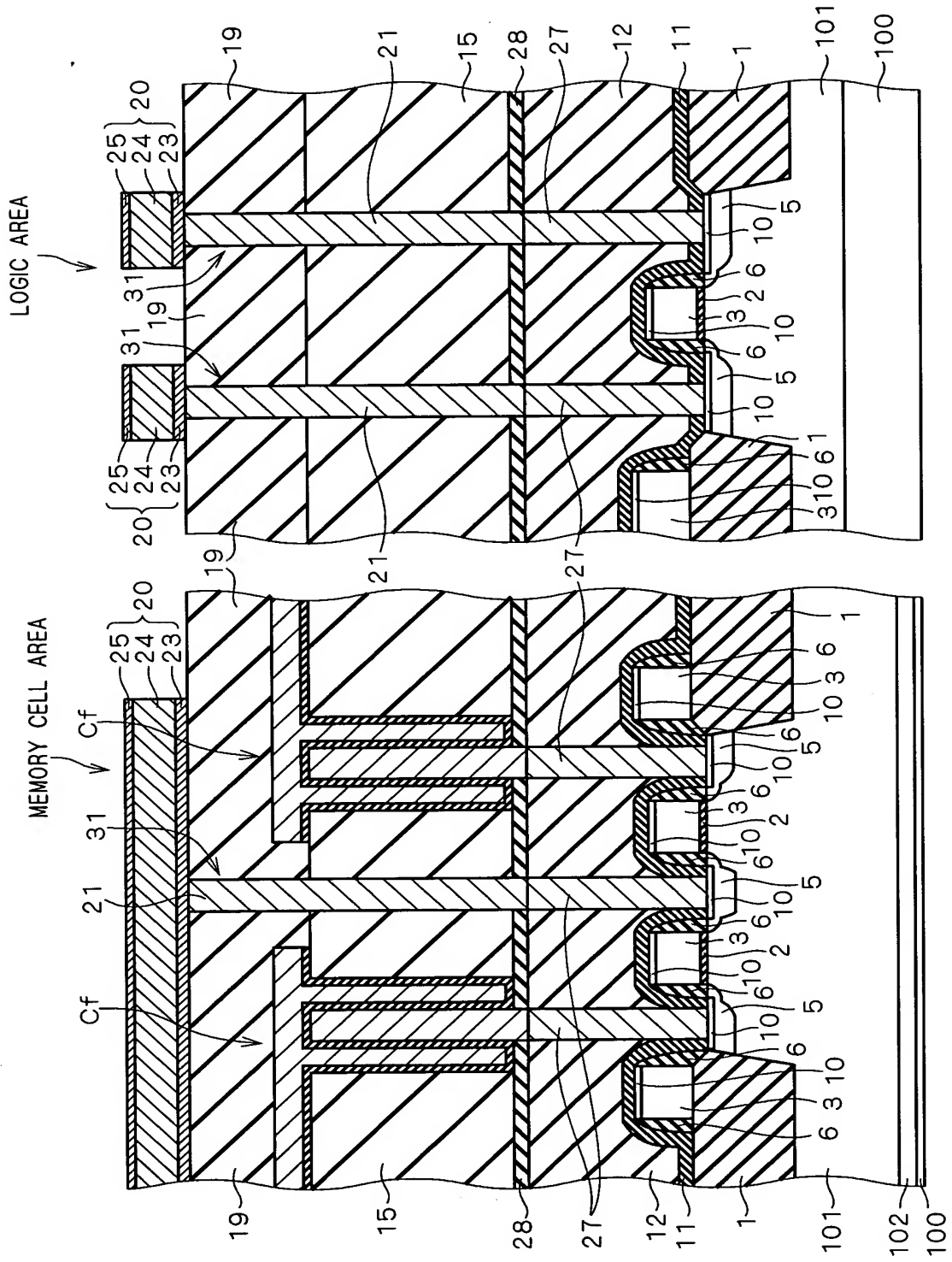


FIG. 49

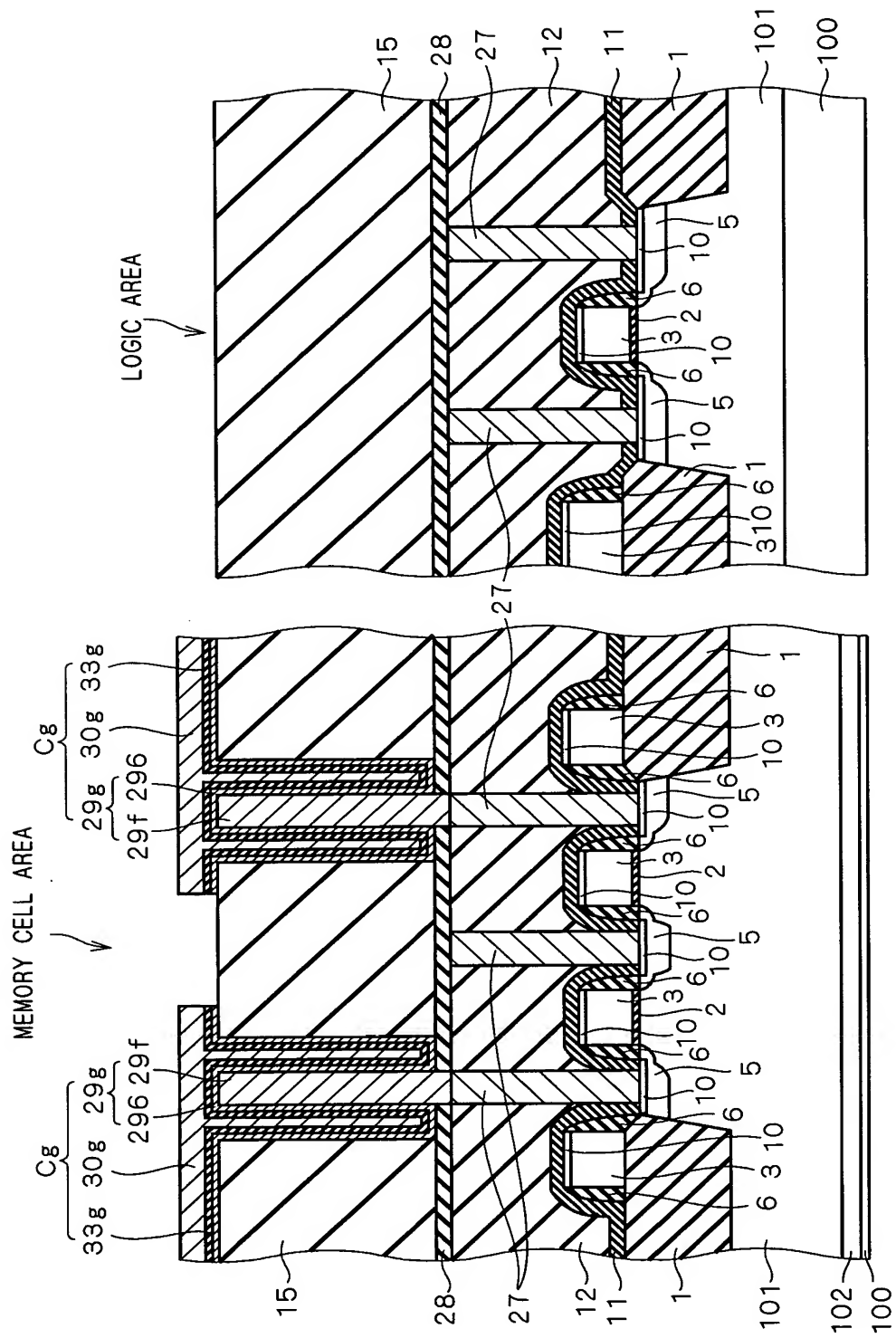
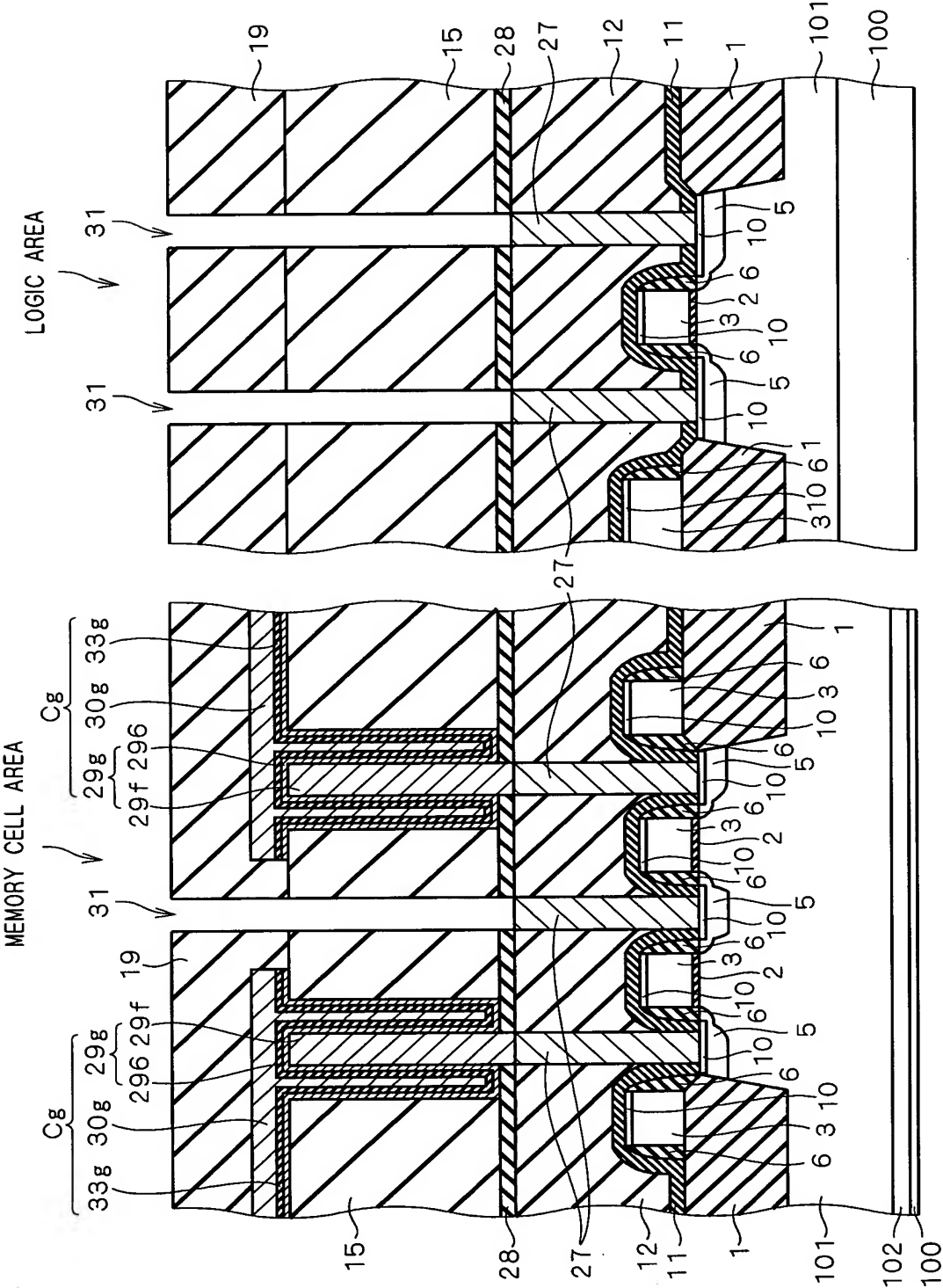
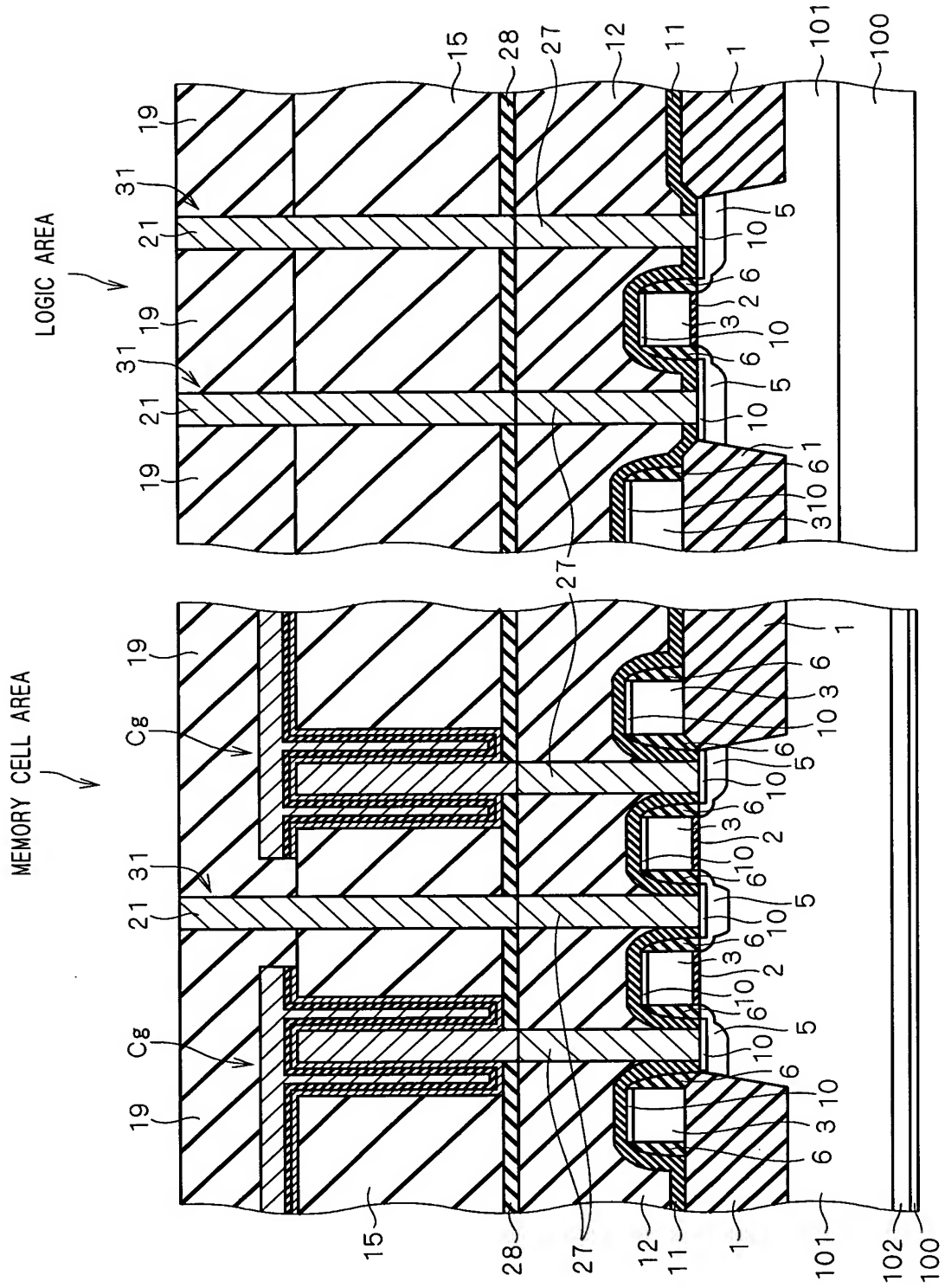


FIG. 50



F I G . 5 1



F I G . 5 2

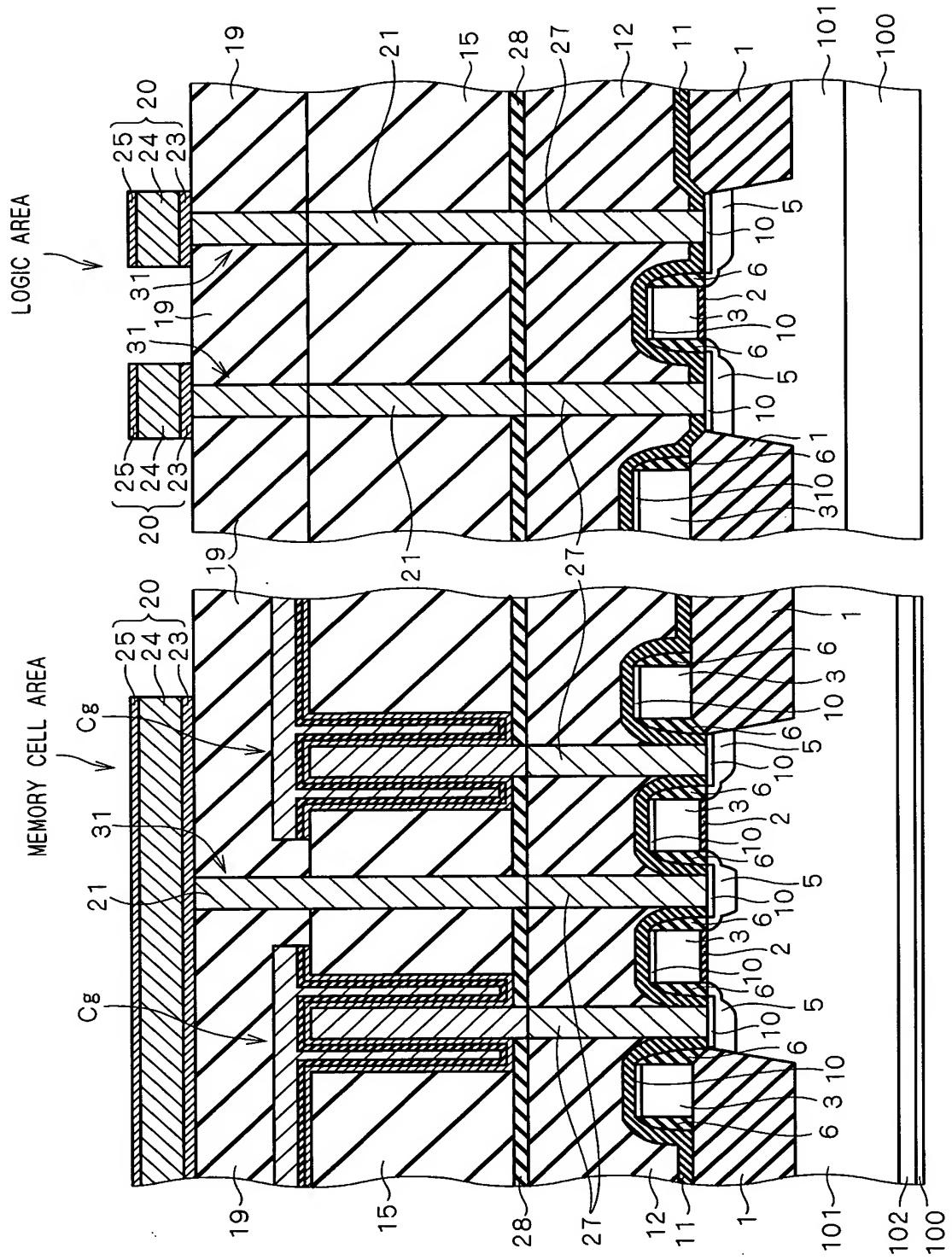
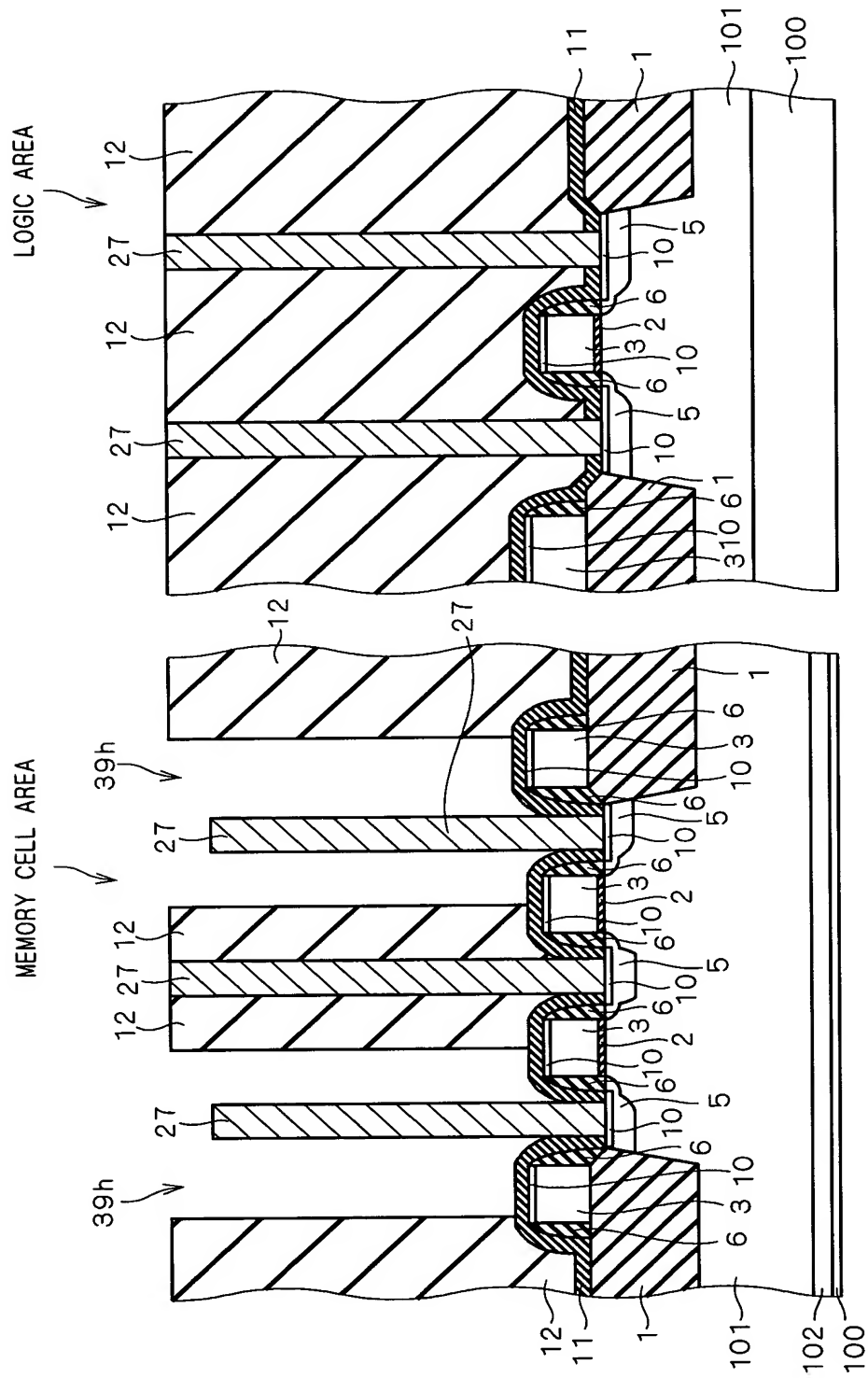
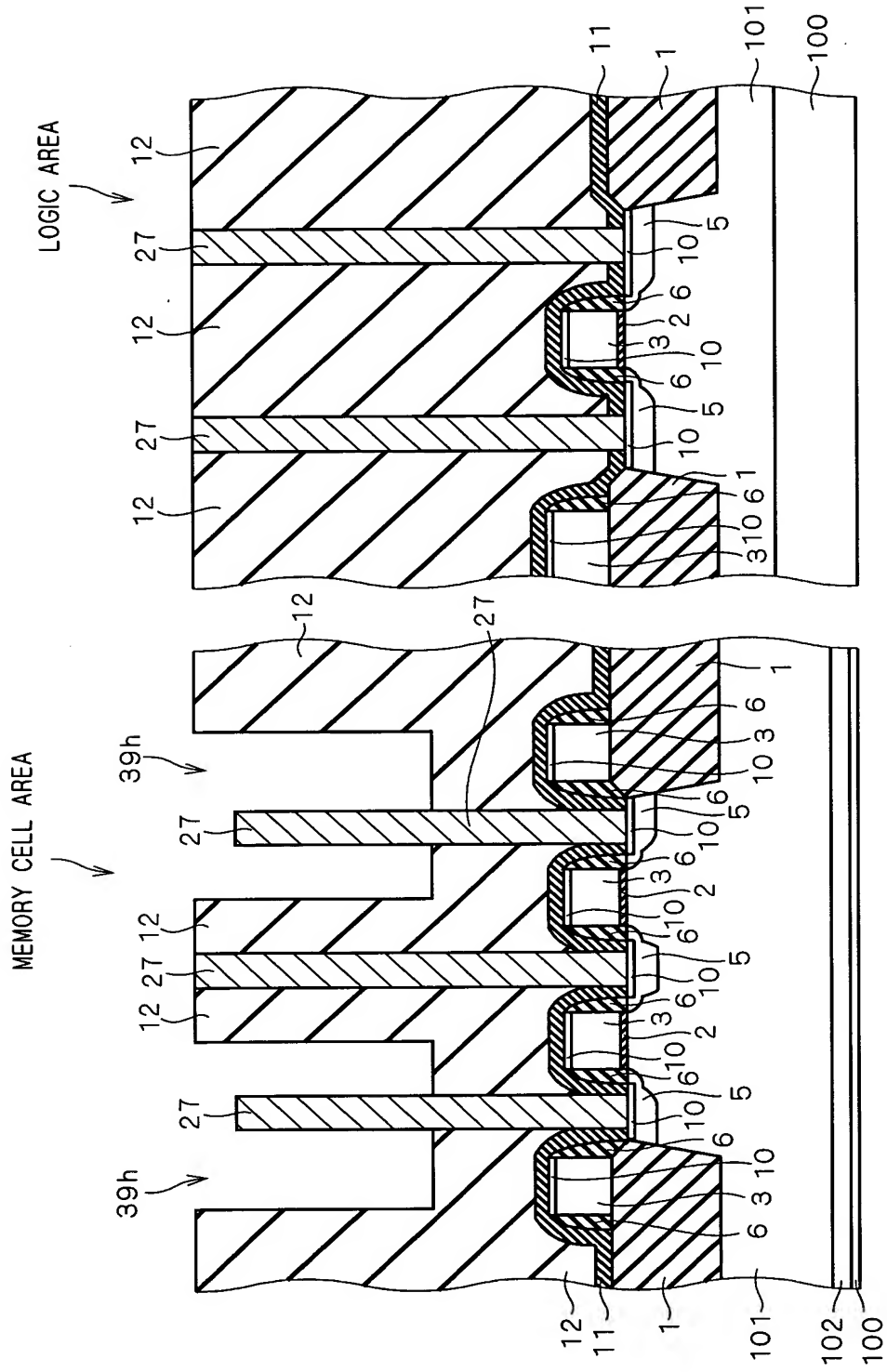


FIG. 53



F I G . 5 4



F I G . 5 5

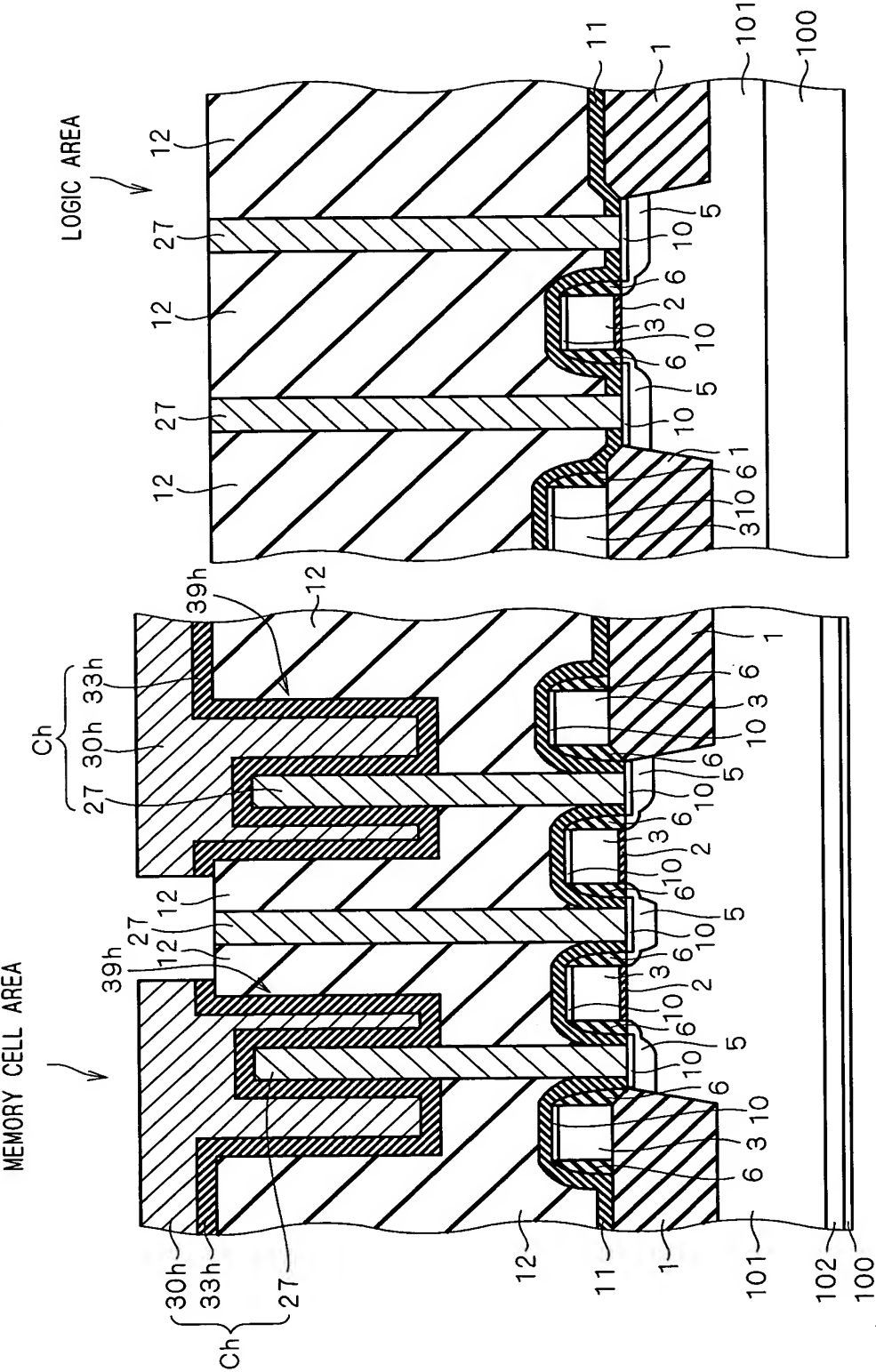


FIG. 56

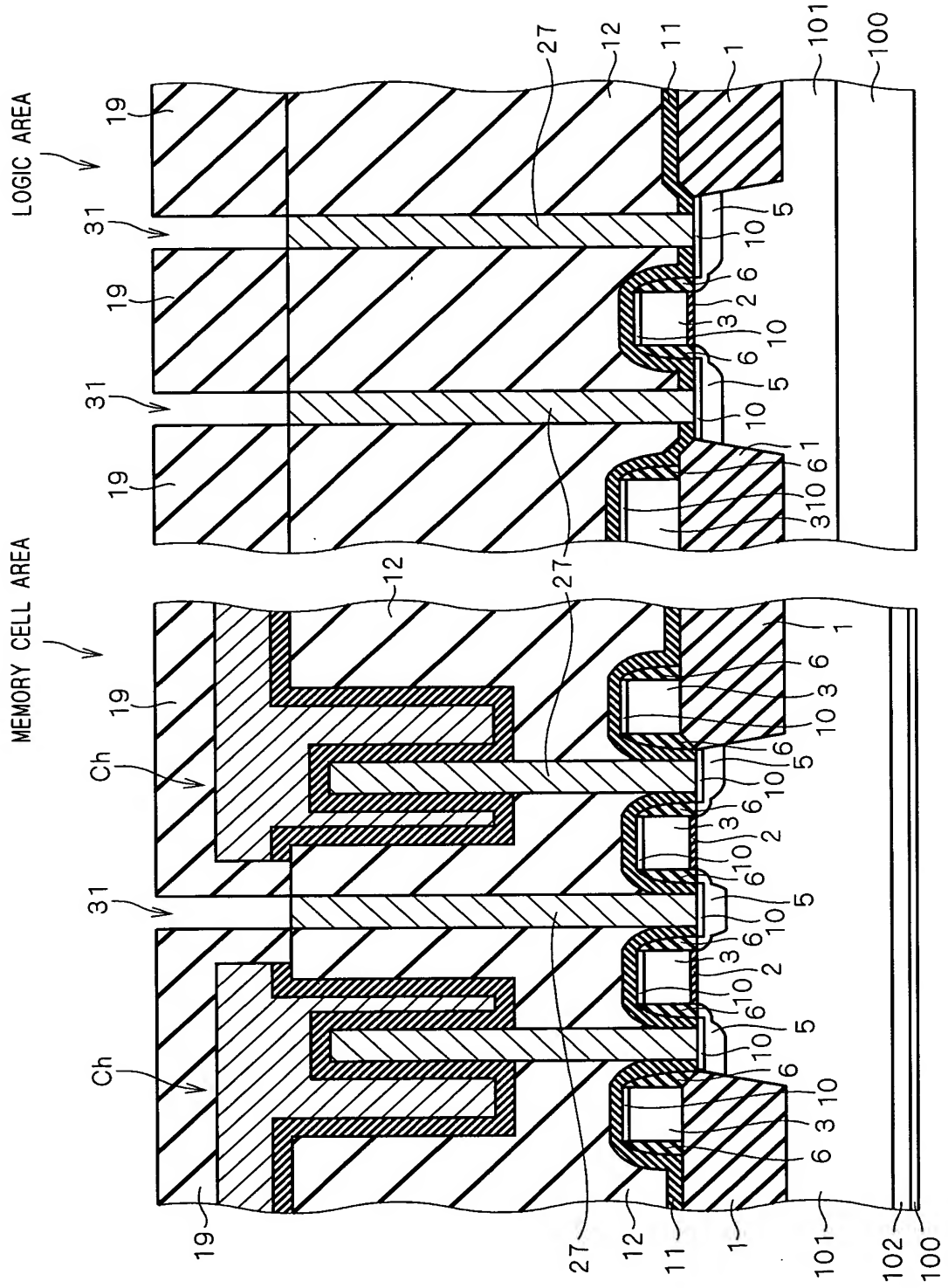
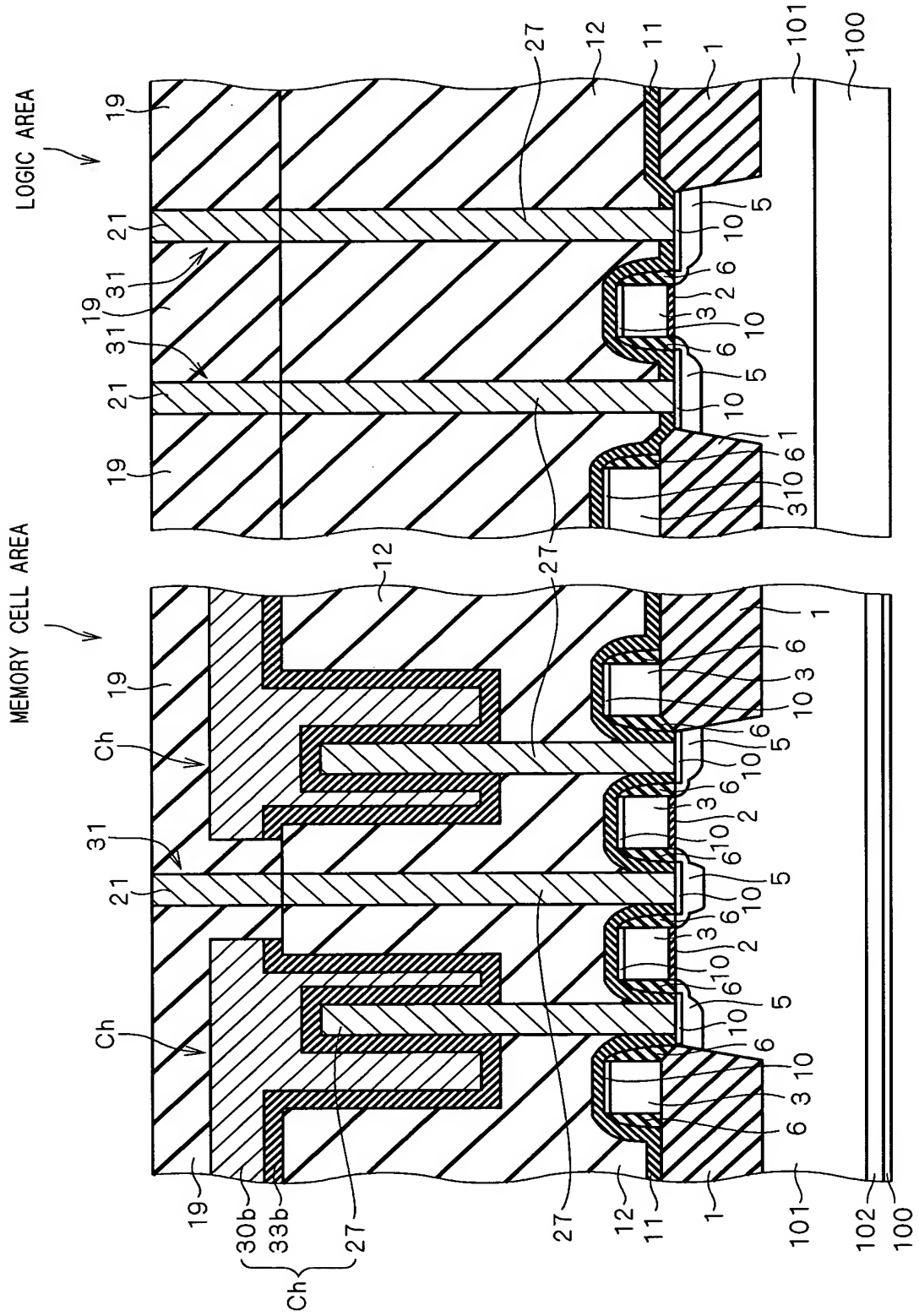


FIG. 57



F I G . 5 8

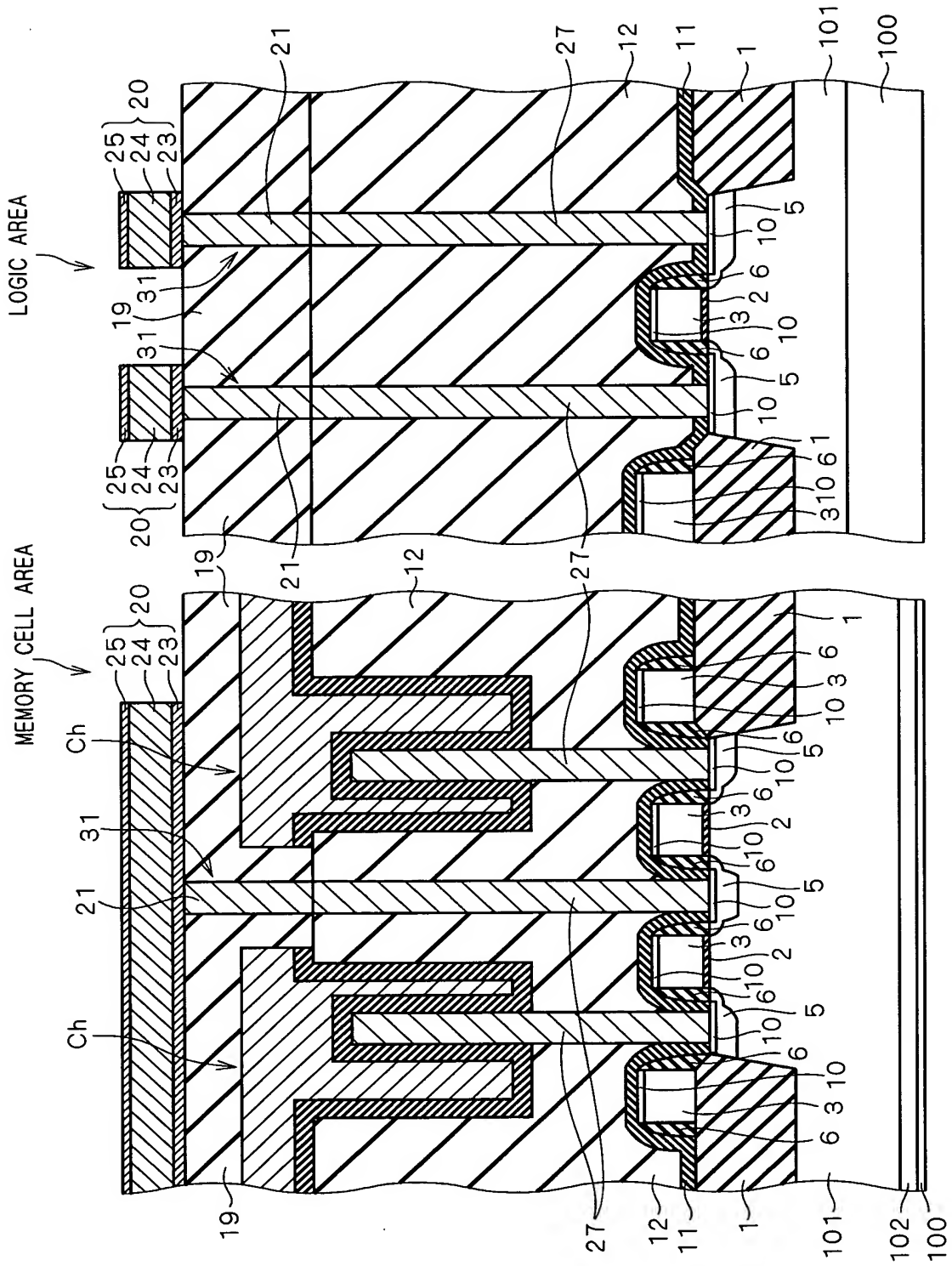


FIG. 59

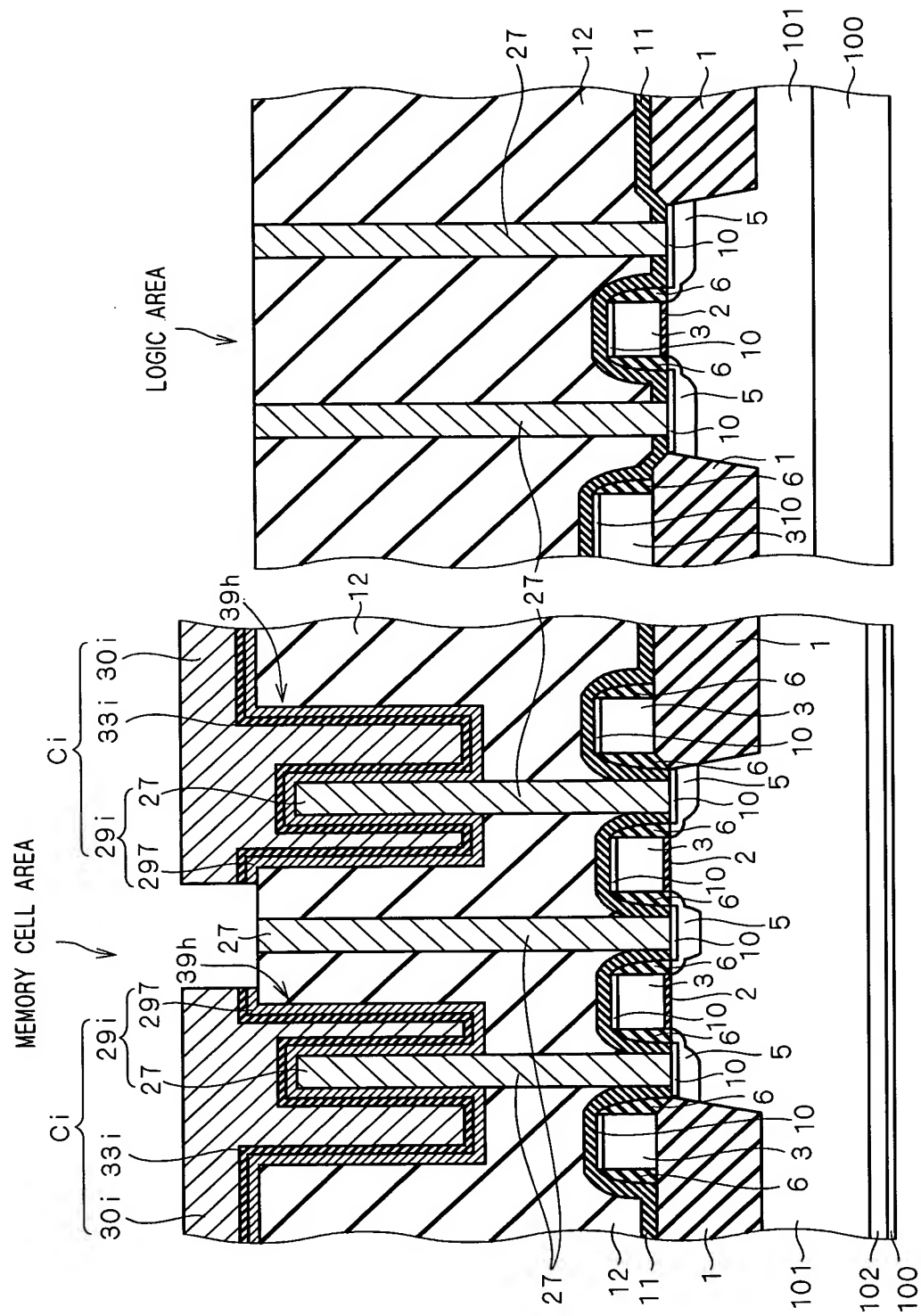
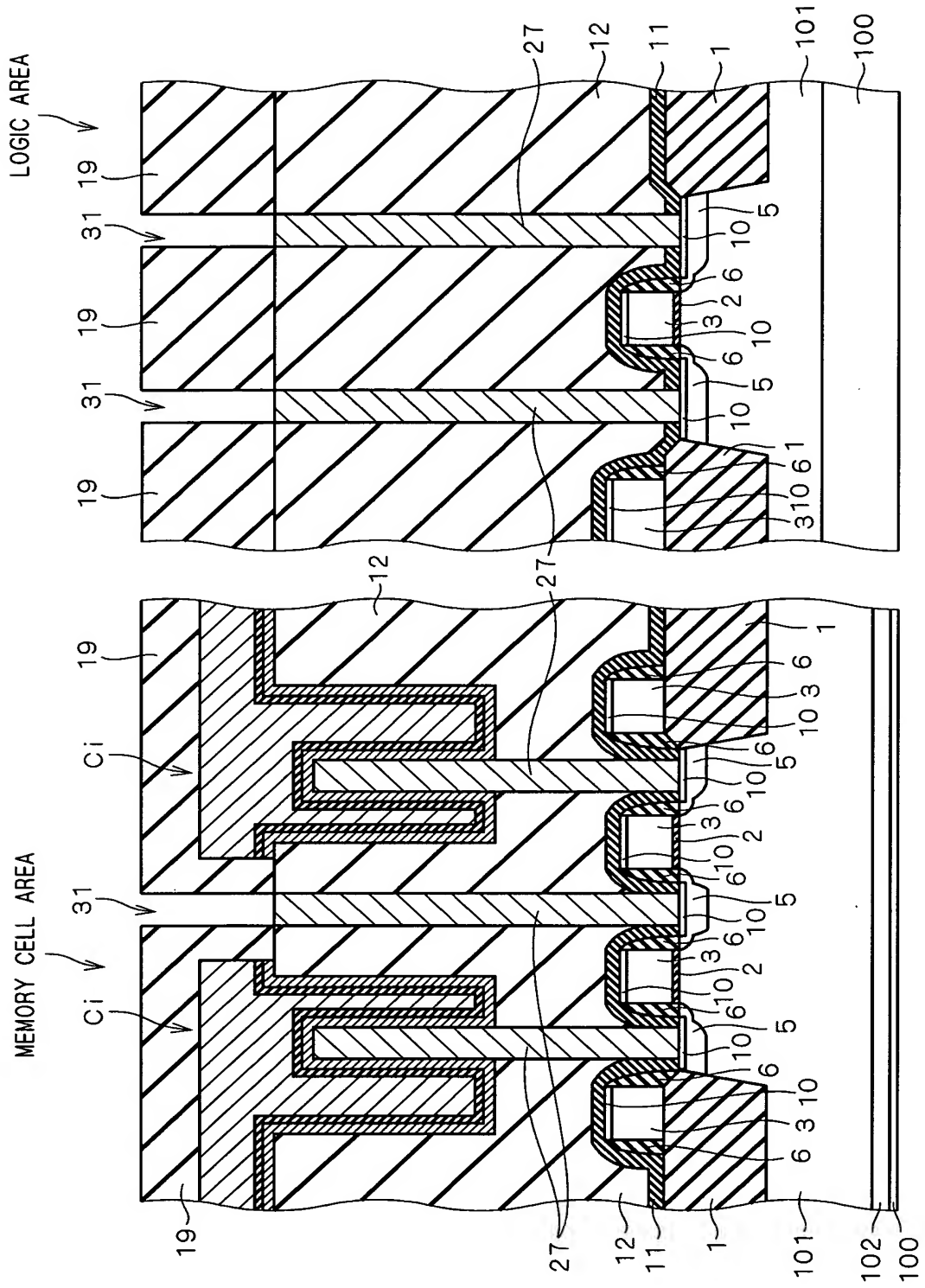
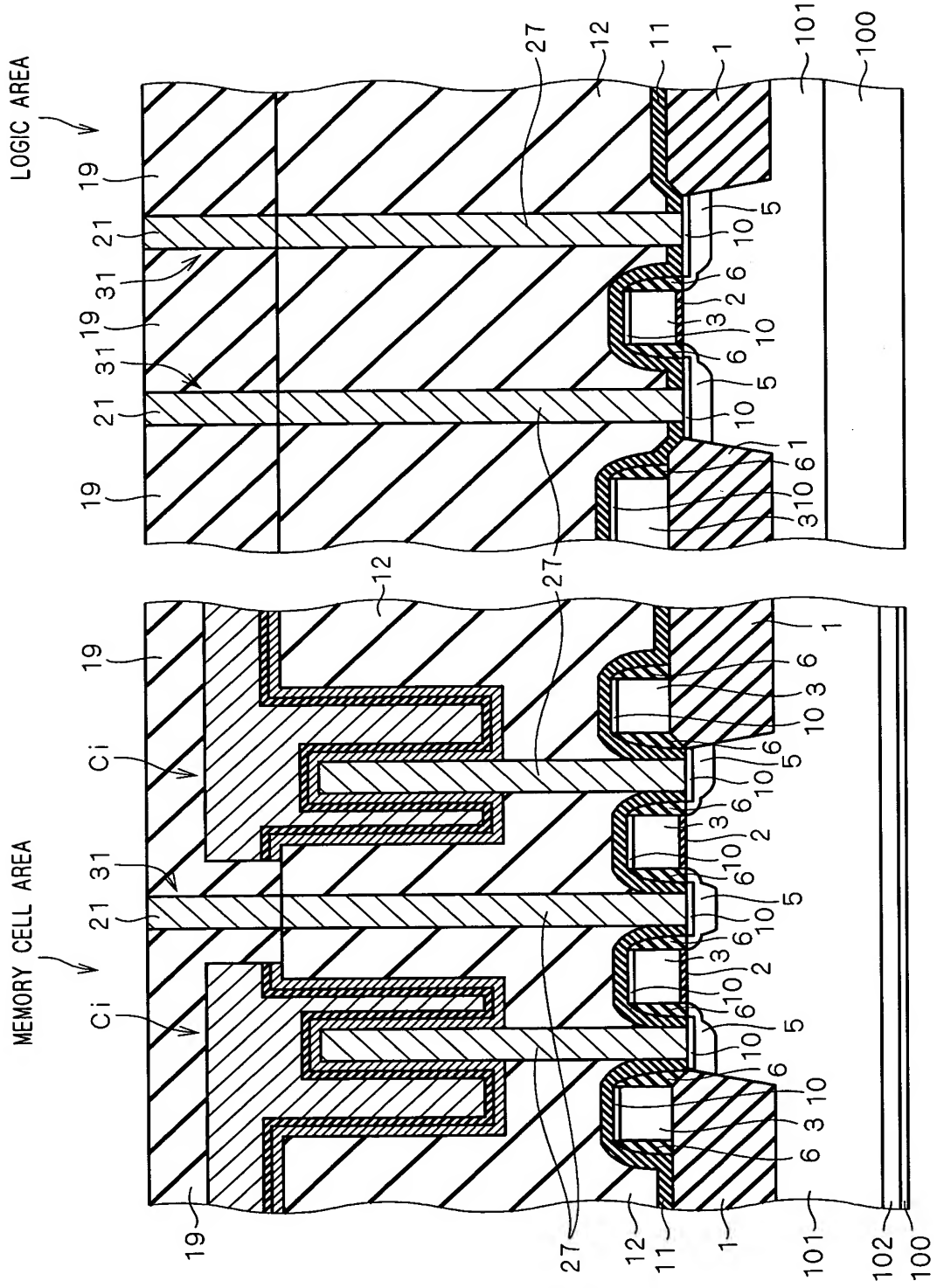


FIG. 60



F I G . 6 1



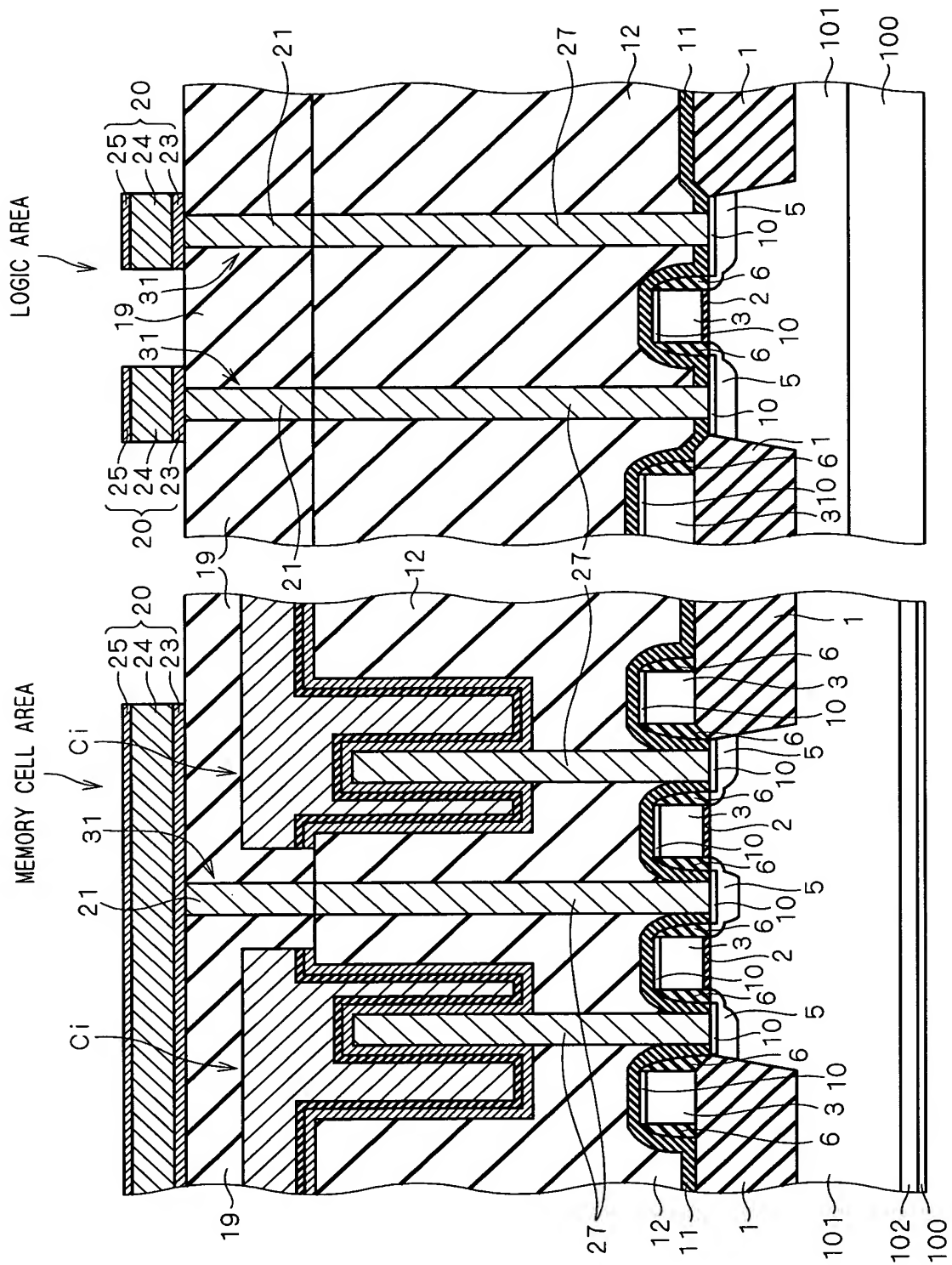
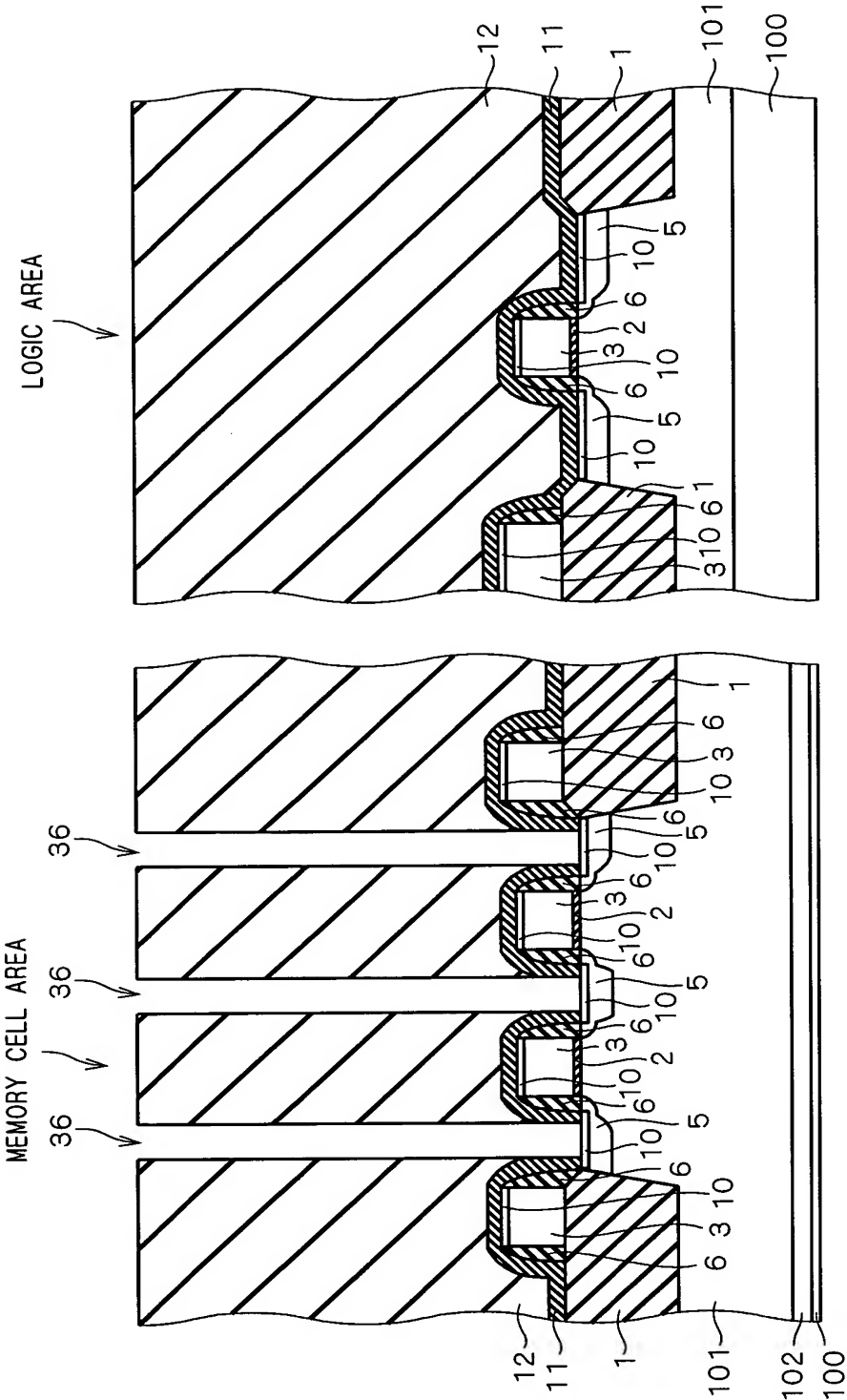
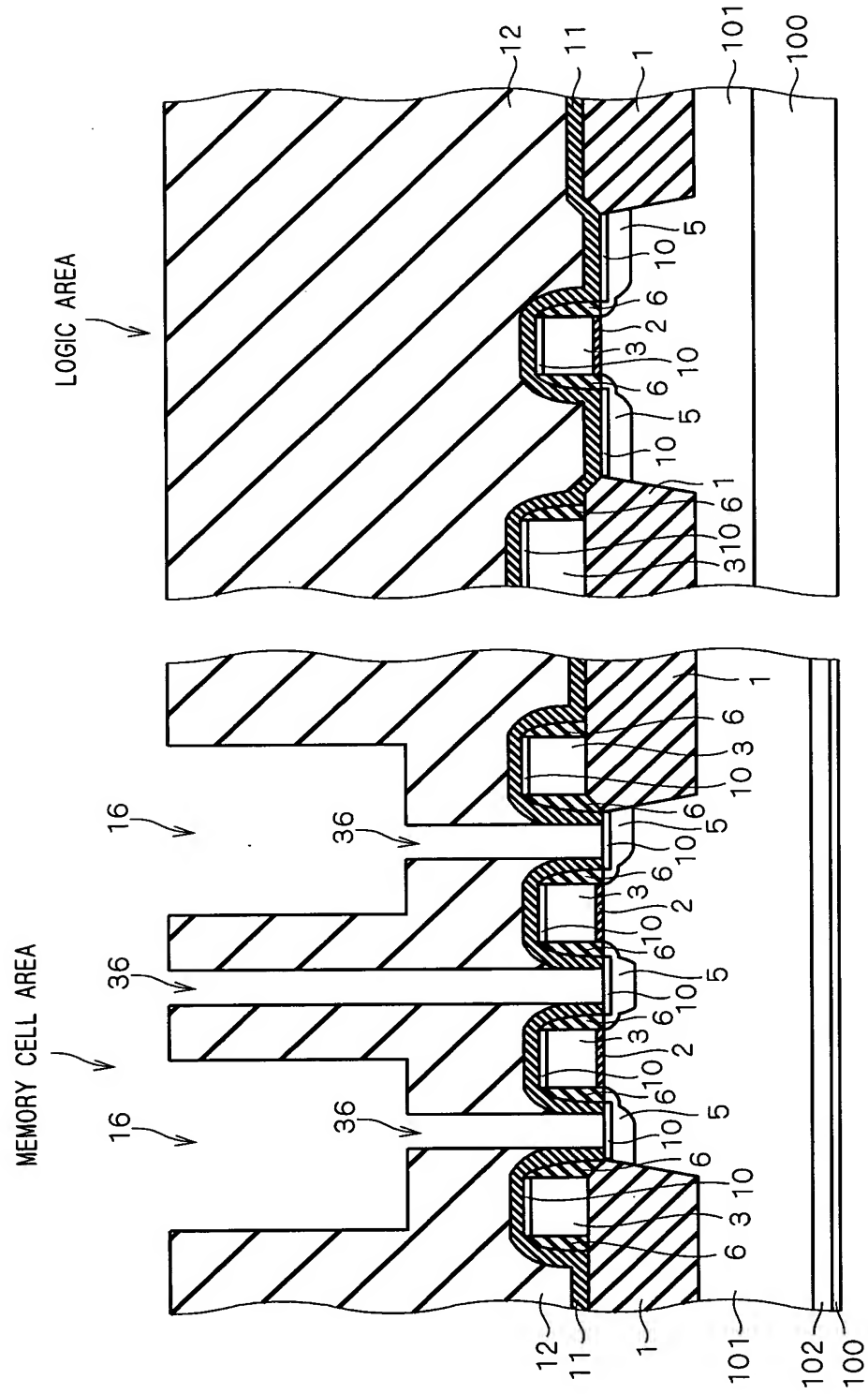


FIG. 63



F I G . 6 4



F I G . 6 5

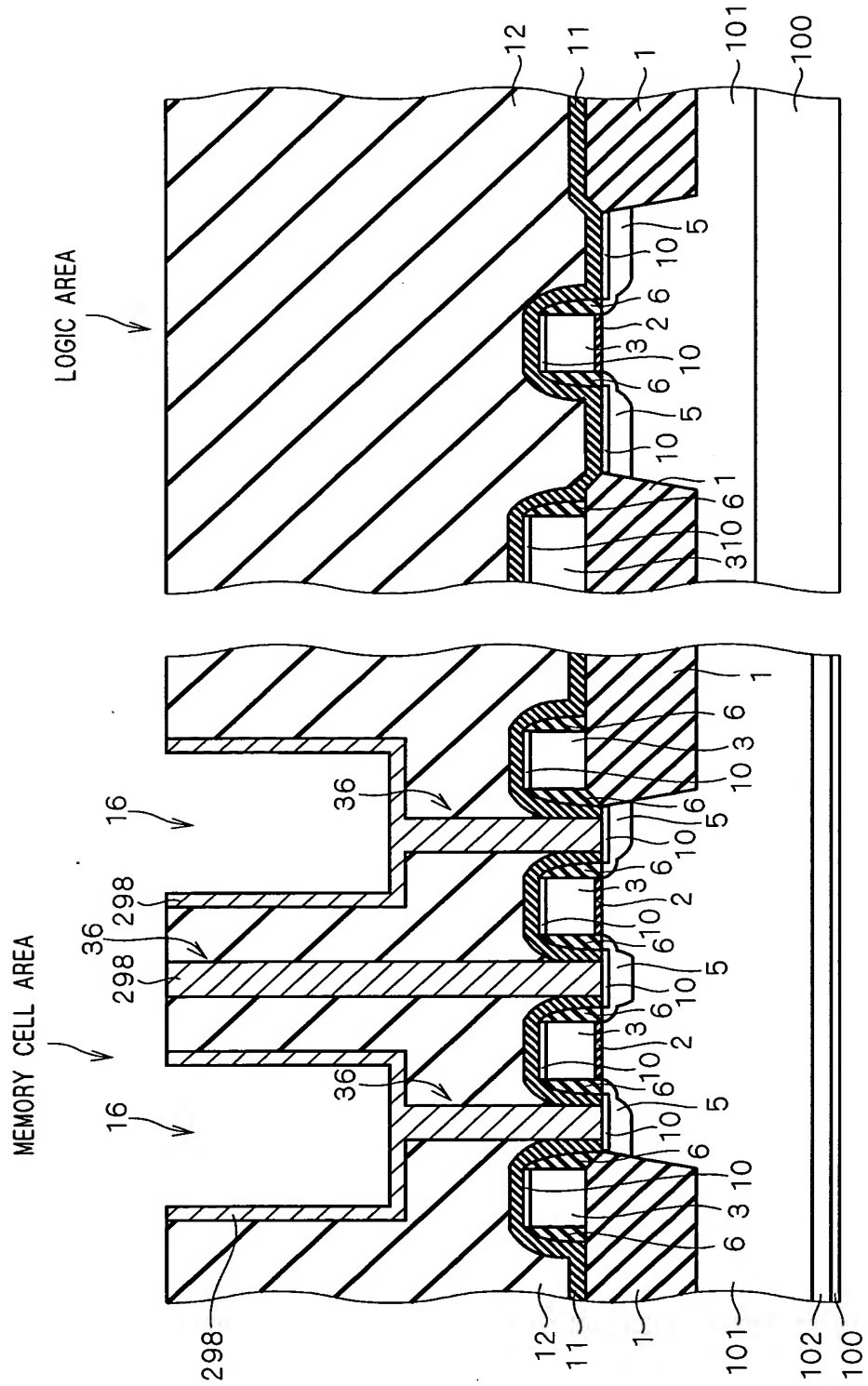


FIG. 66

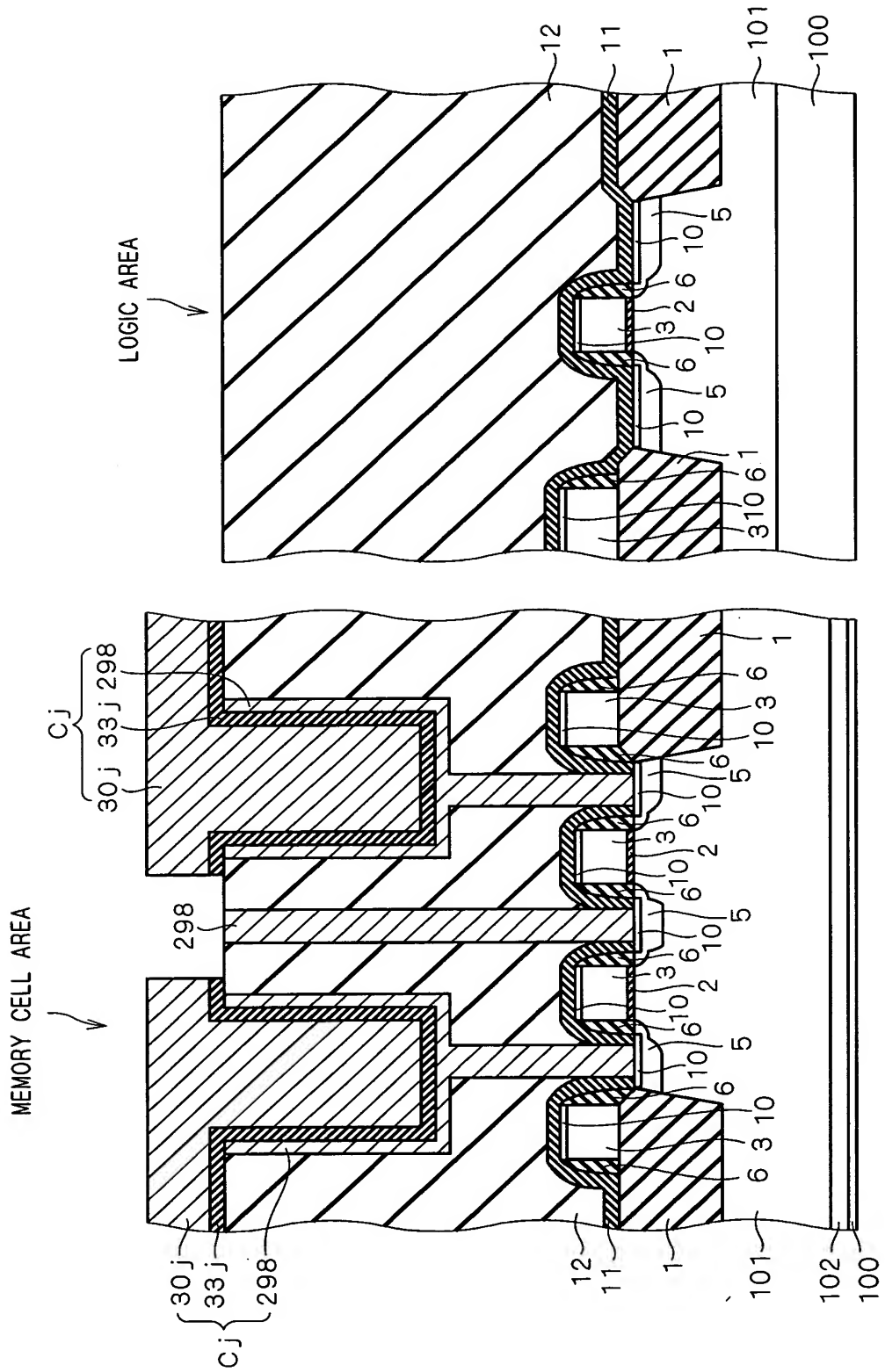
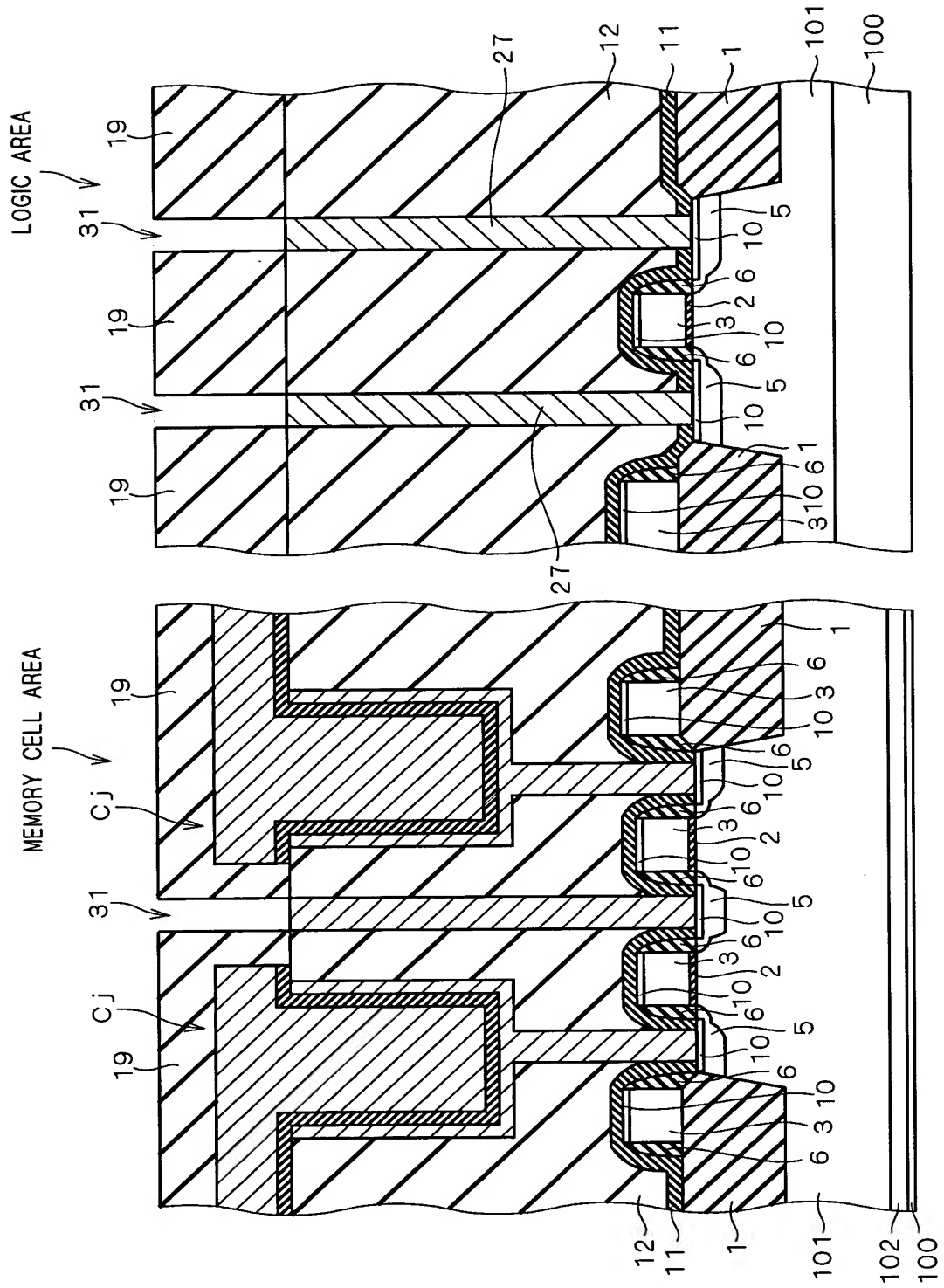
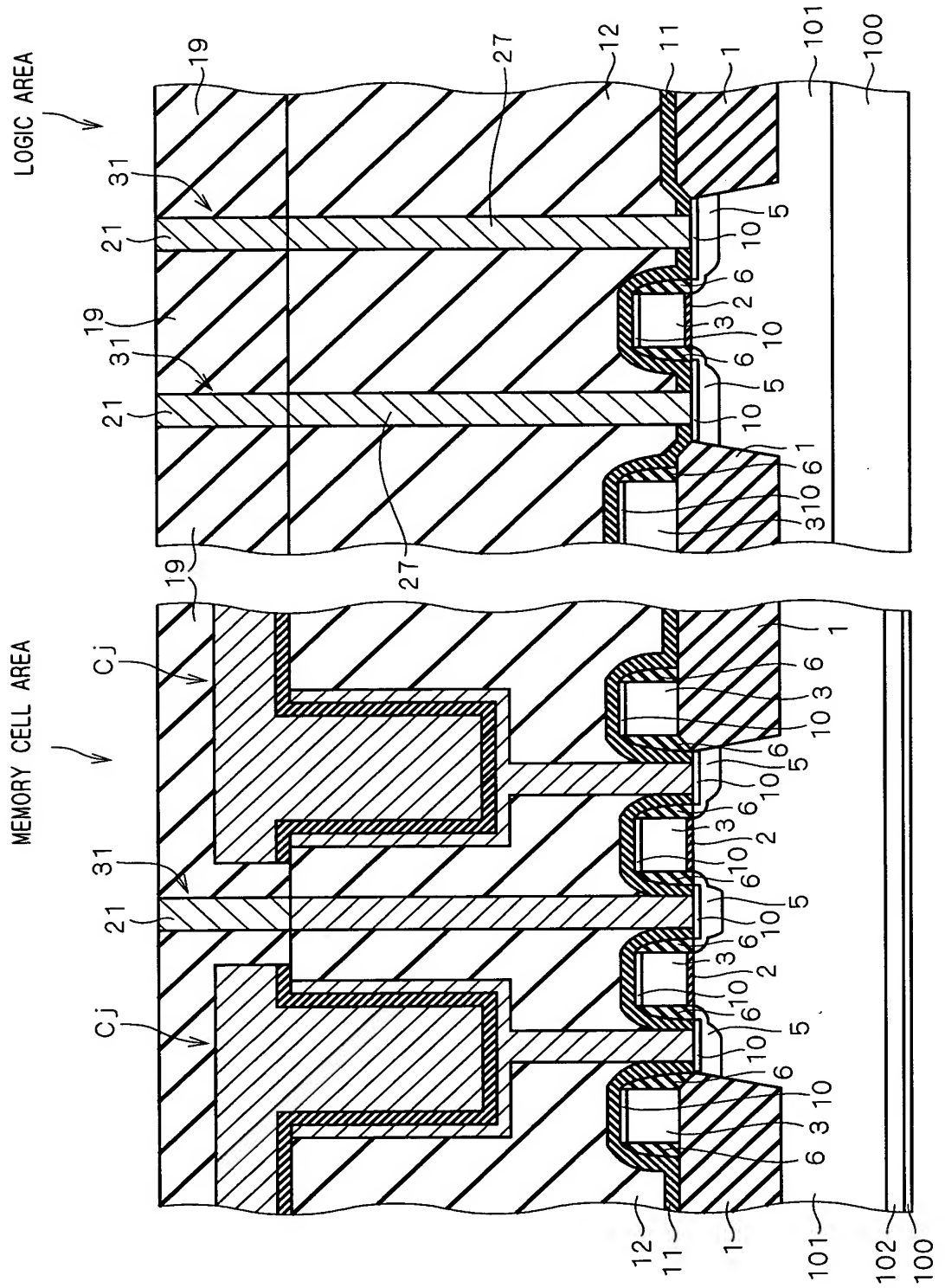


FIG. 67



F I G . 6 8



F I G . 6 9

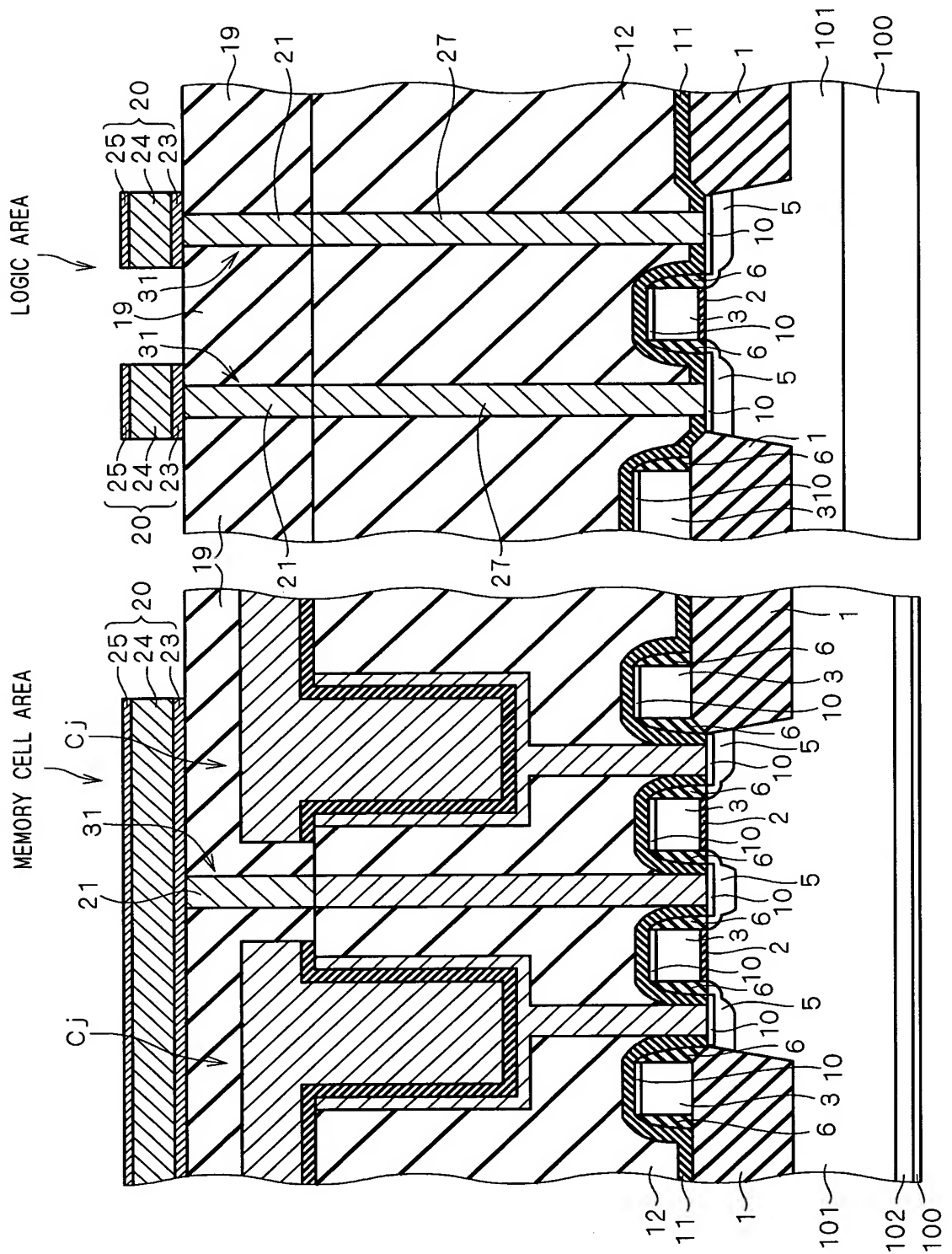
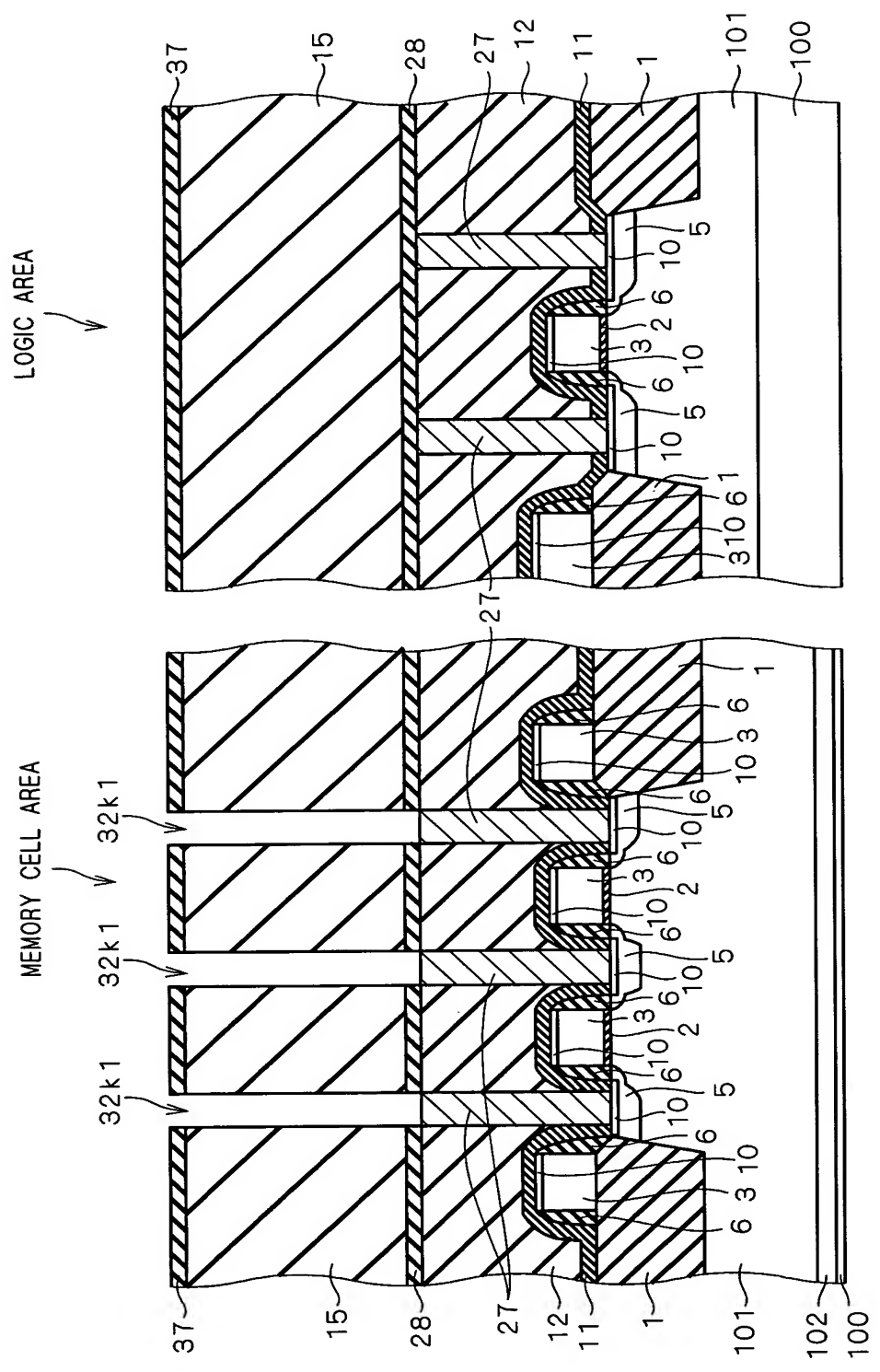
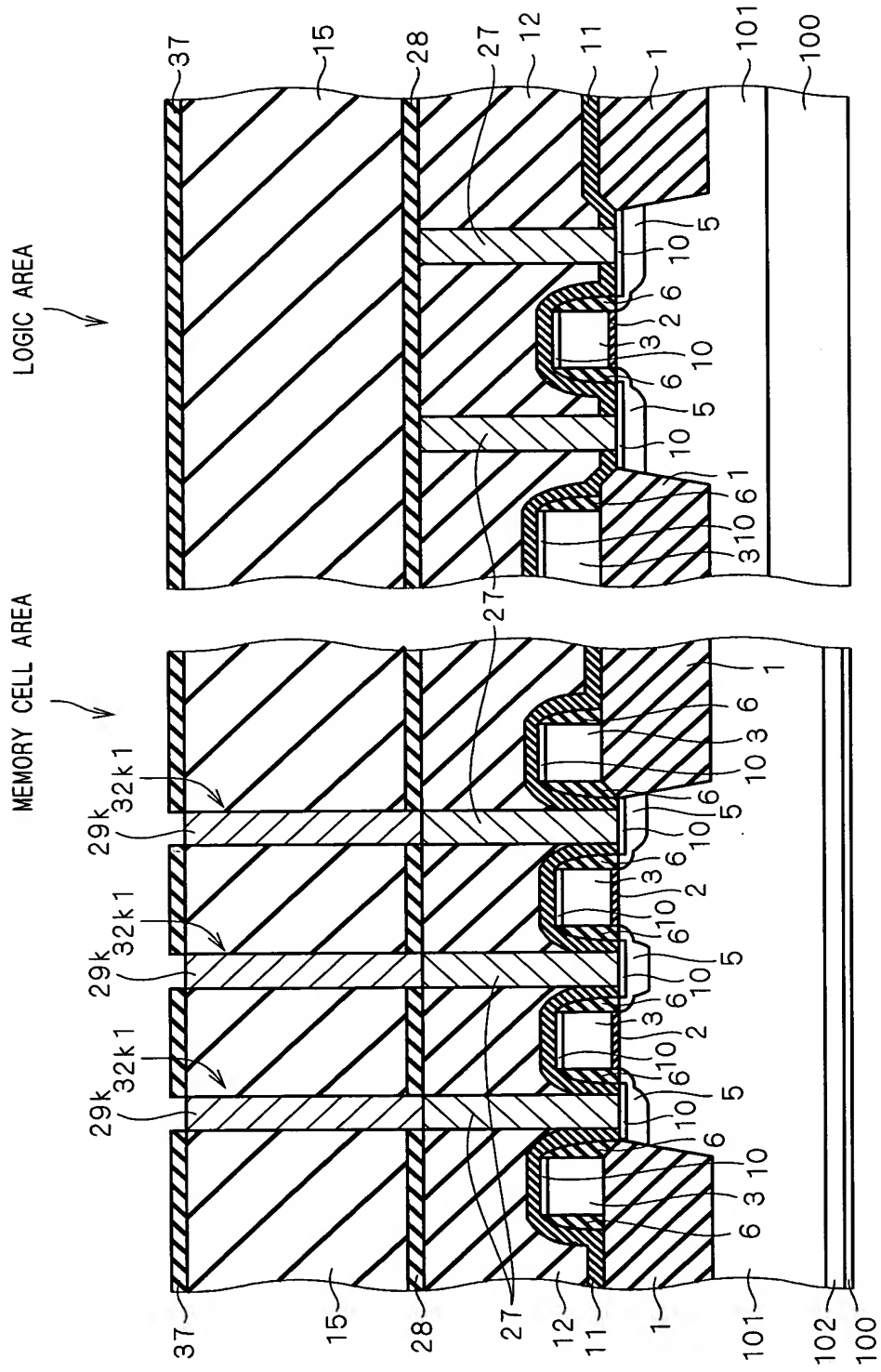


FIG. 70



F I G . 7 1



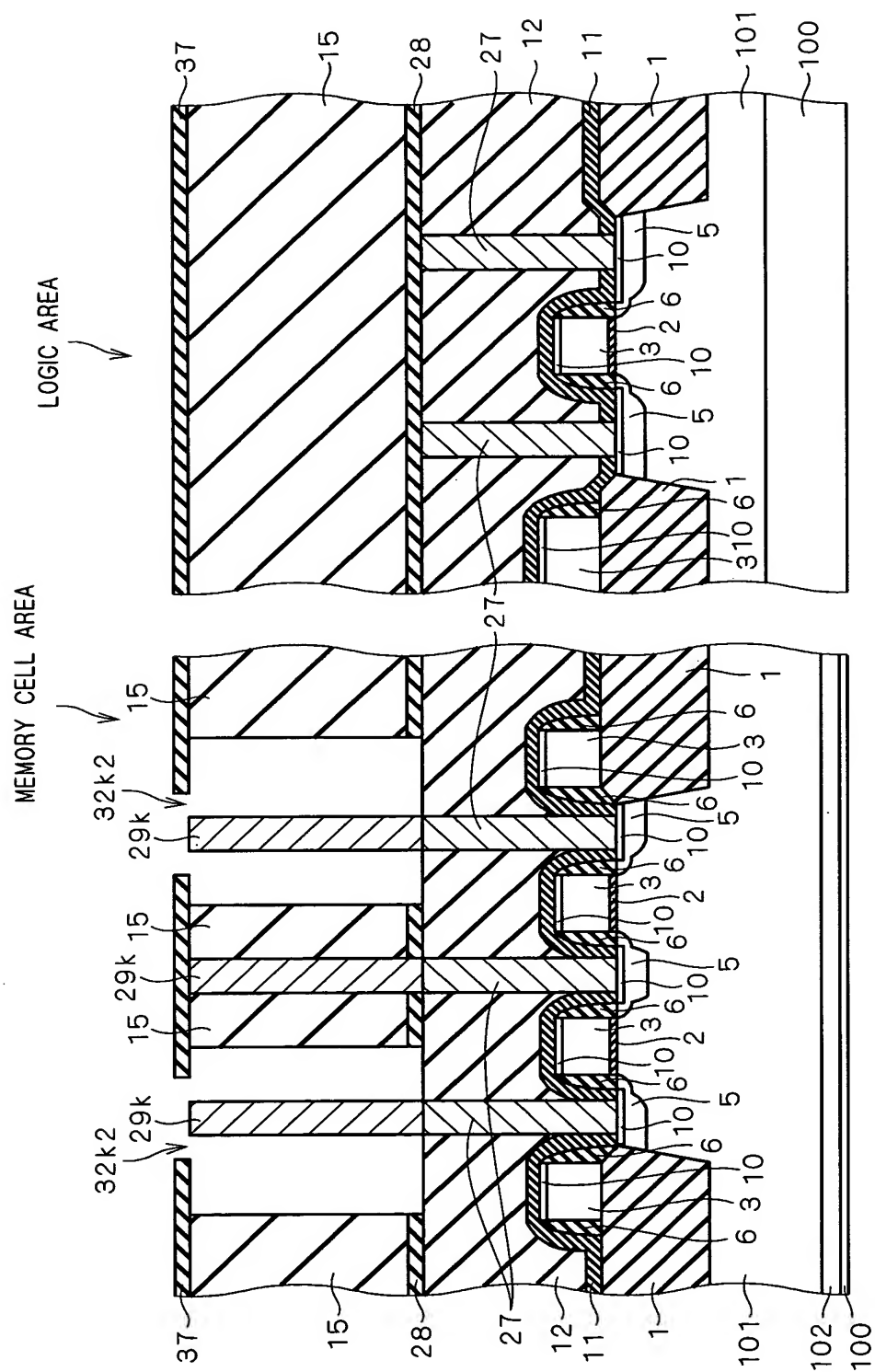
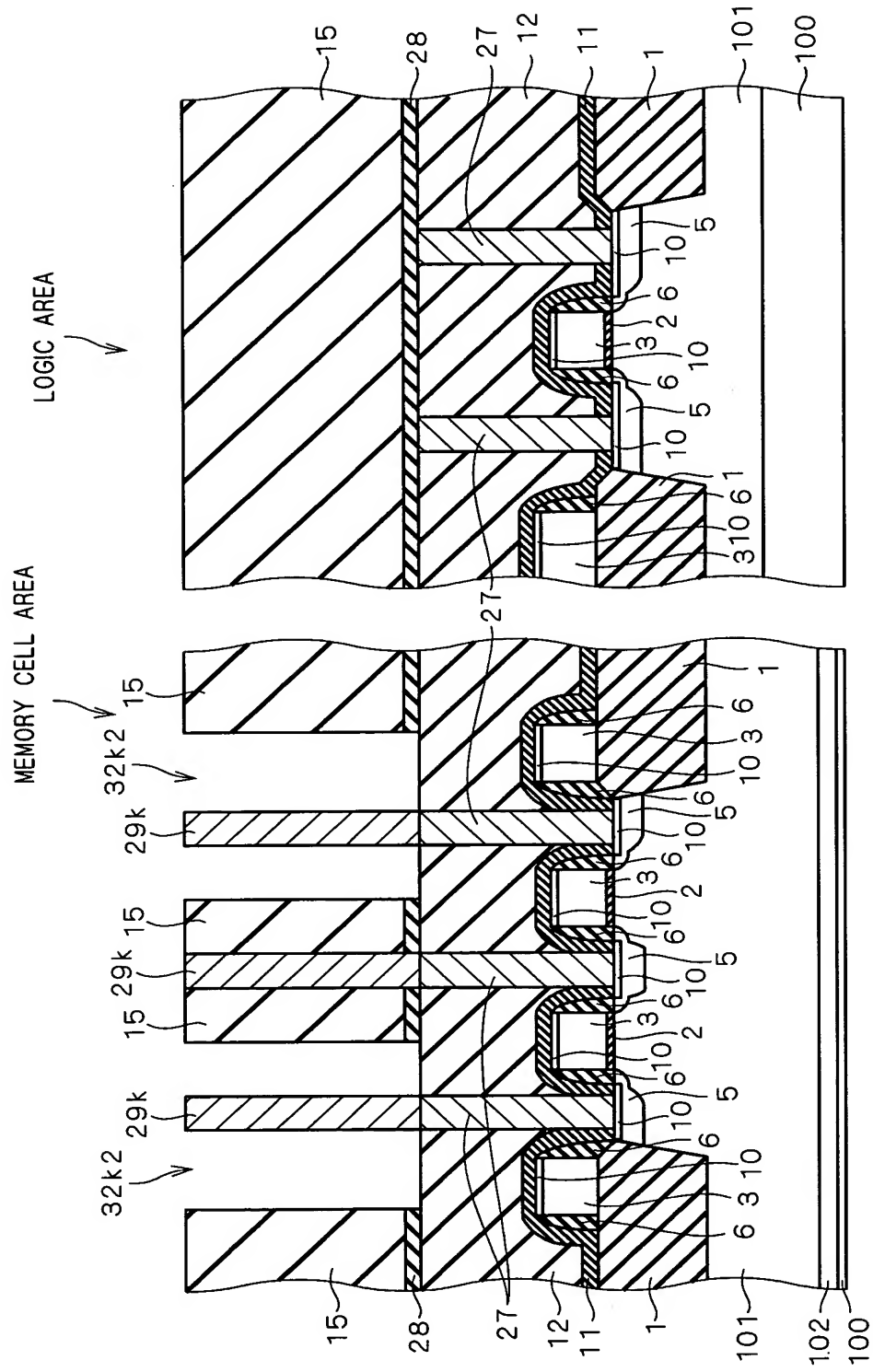


FIG. 73



F I G . 7 4

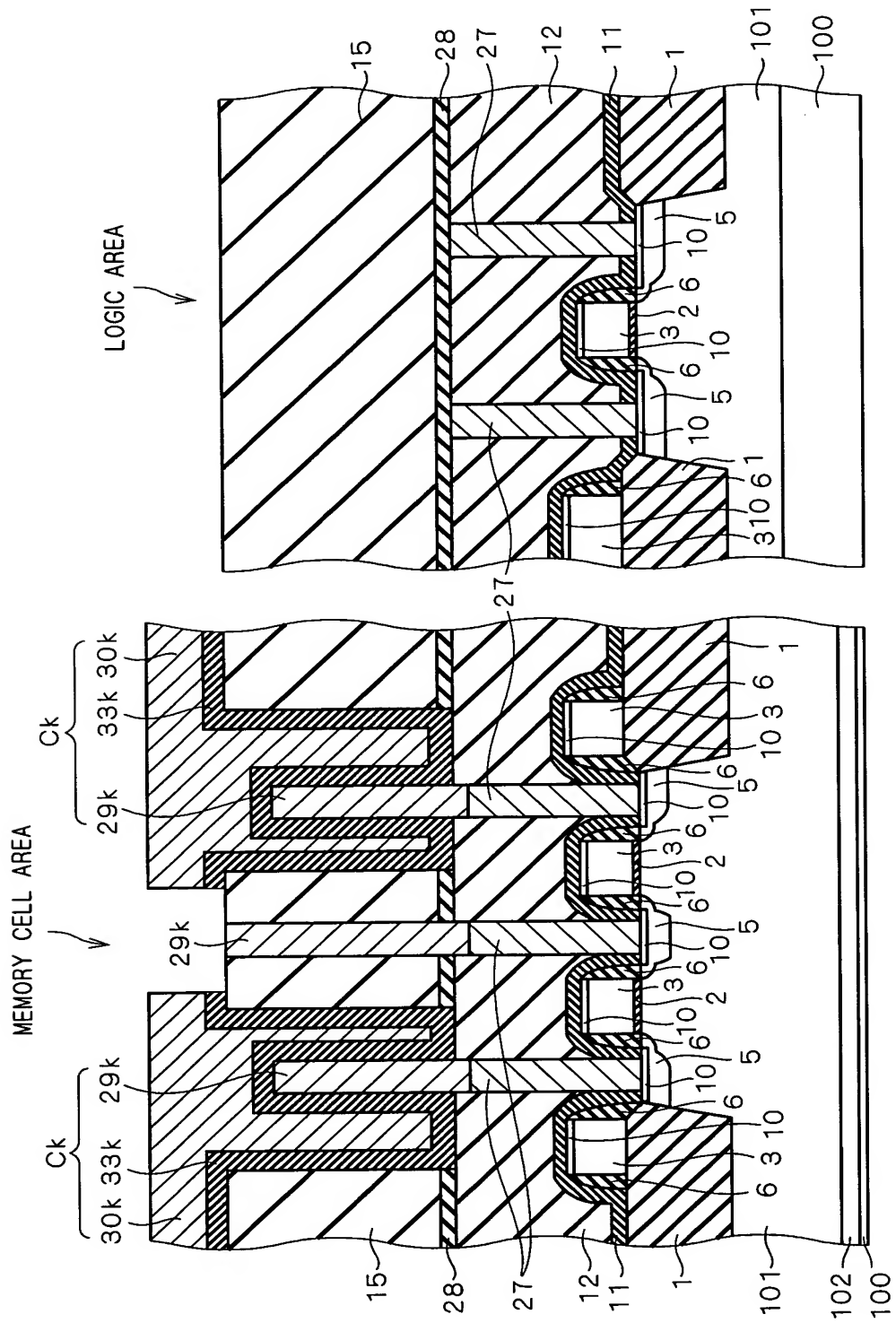
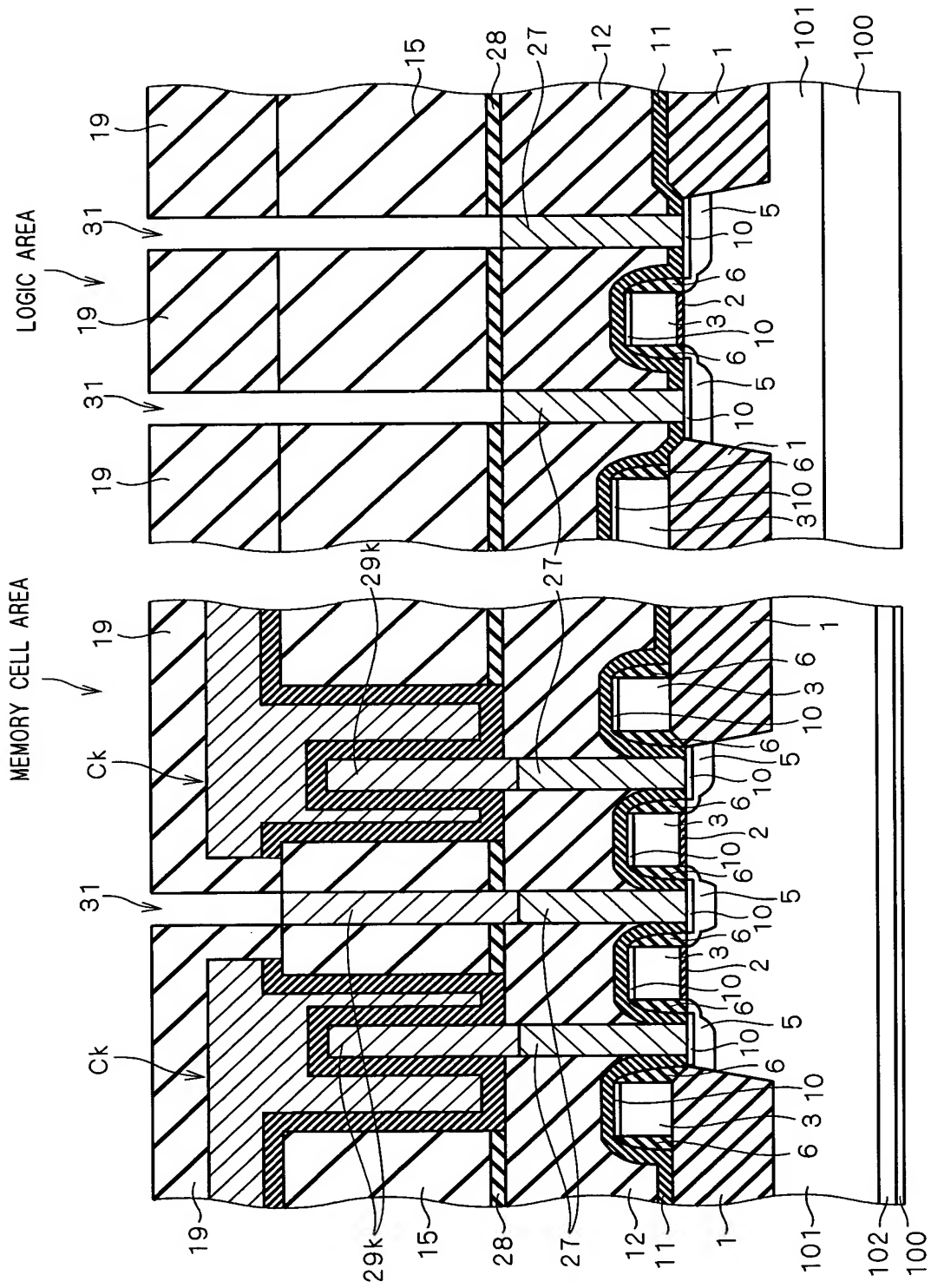
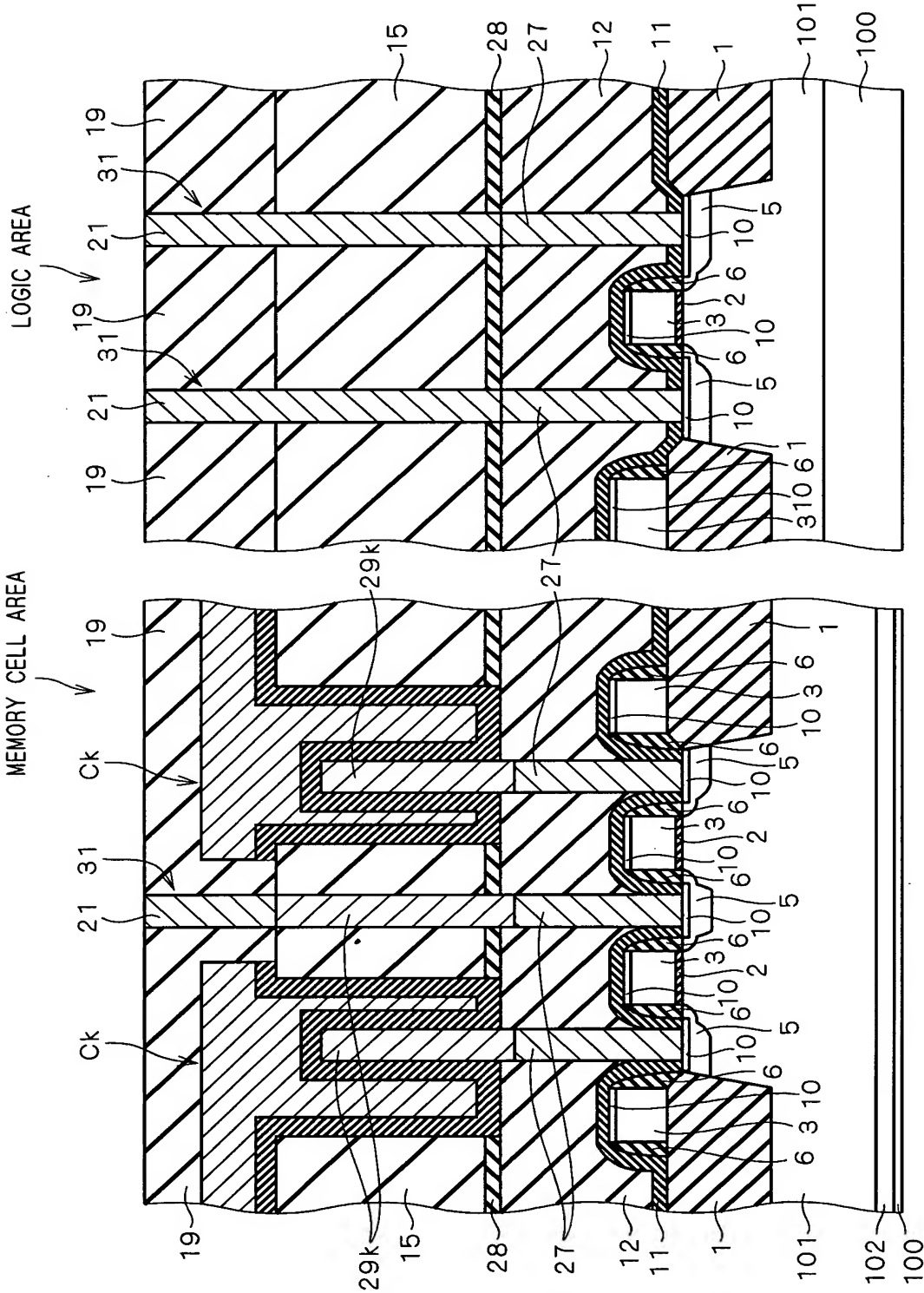


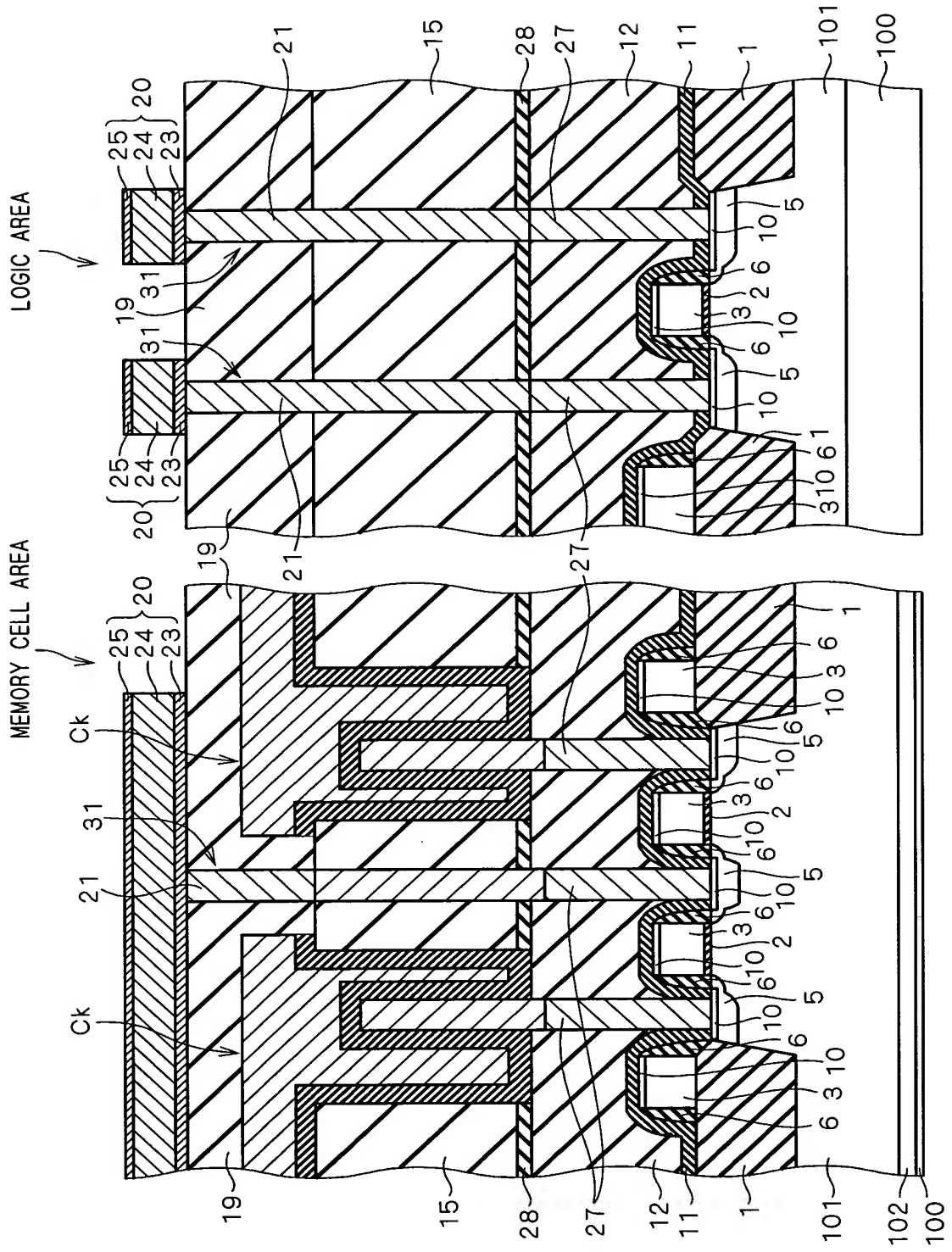
FIG. 75



F I G . 7 6



F I G . 7 7



F I G . 7 8

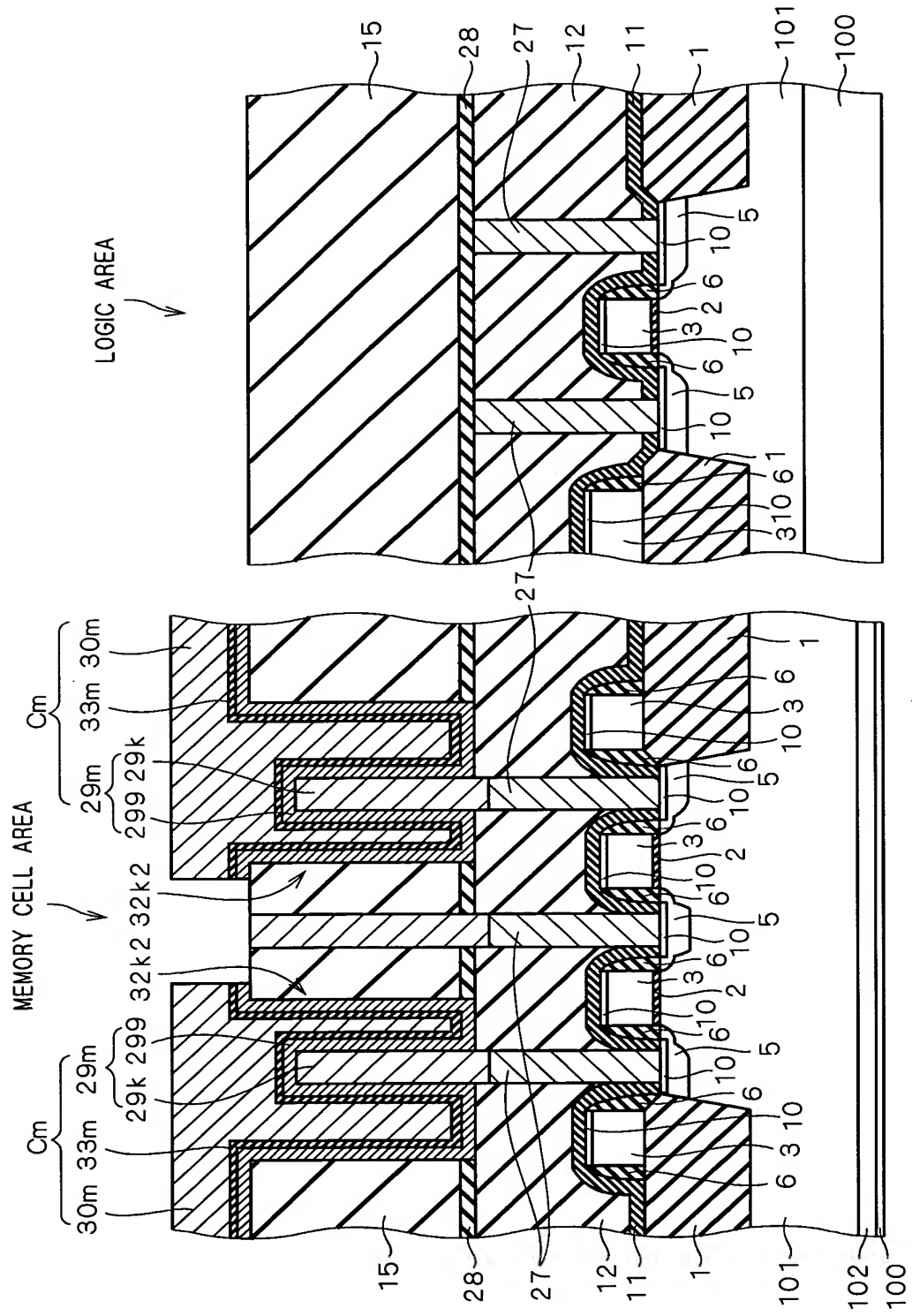
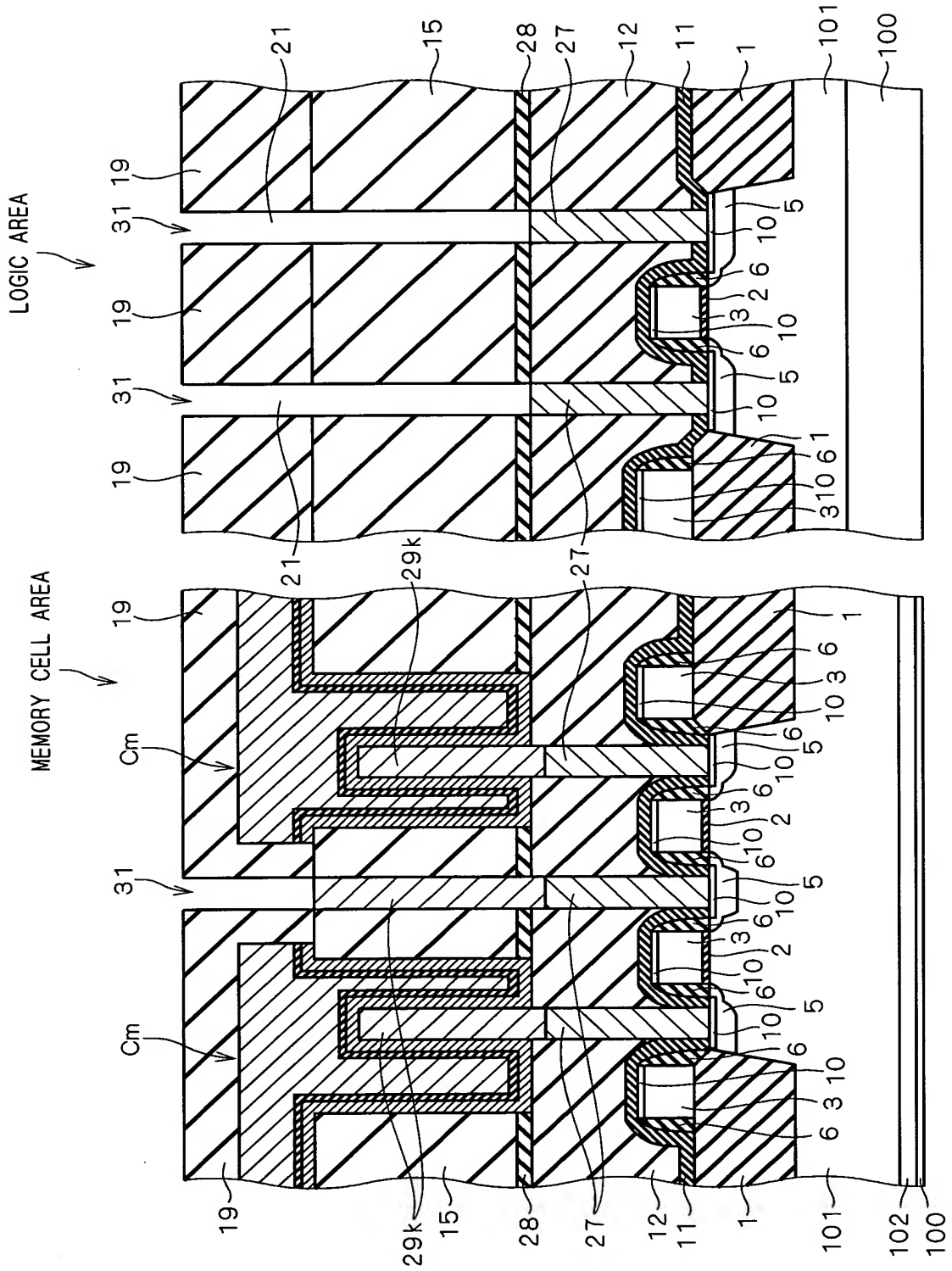
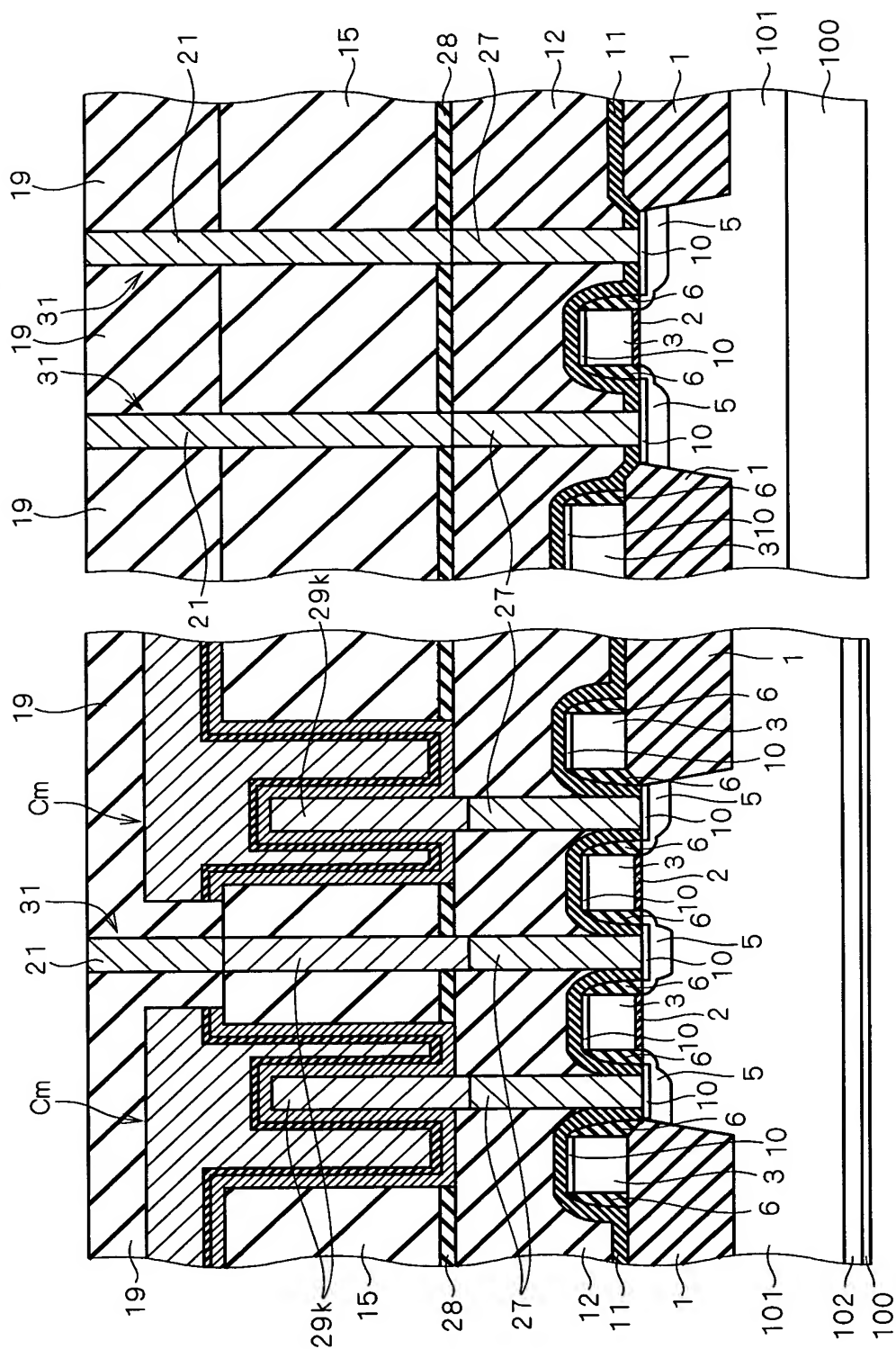


FIG. 79



LOGIC AREA



F I G . 8 1

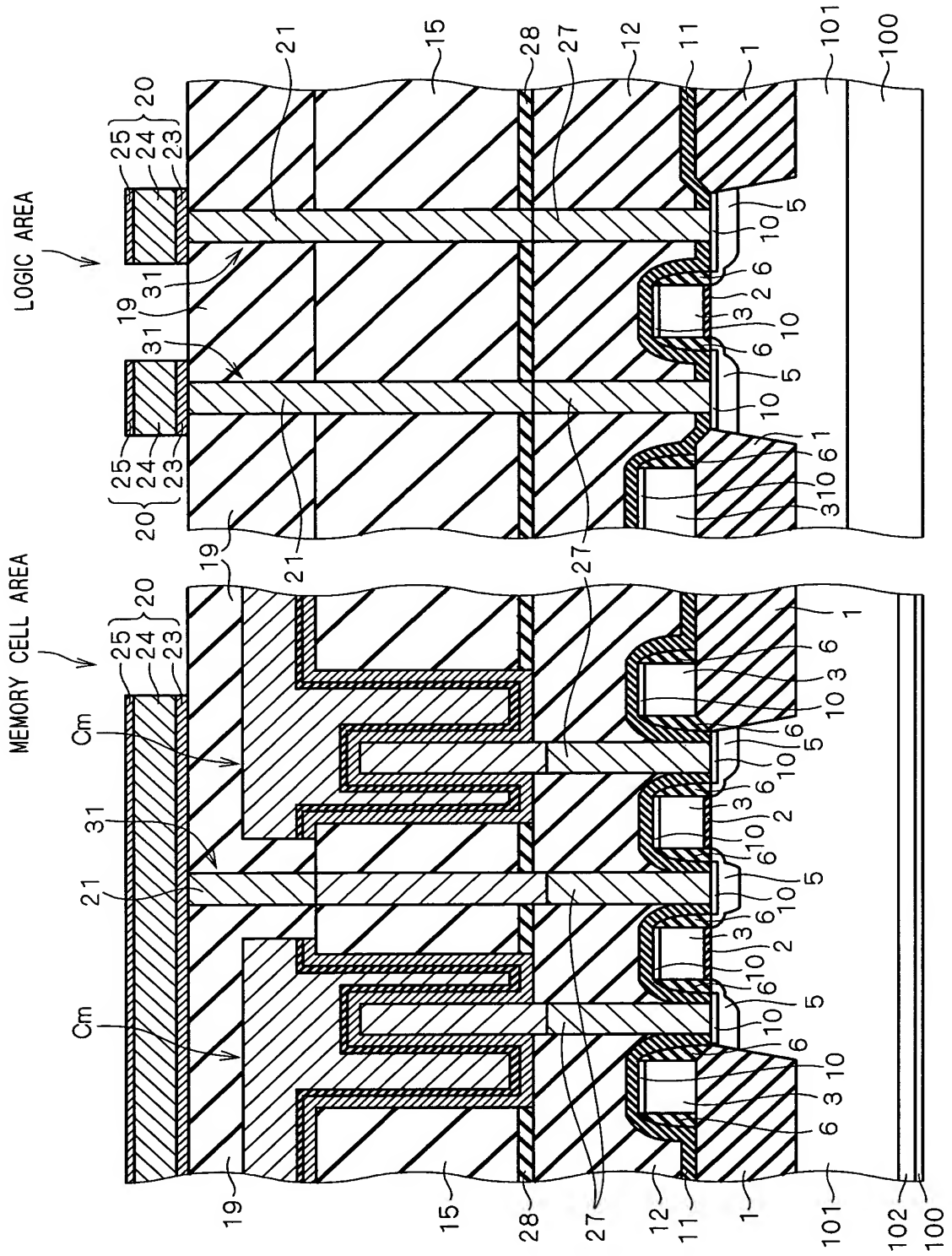


FIG. 82

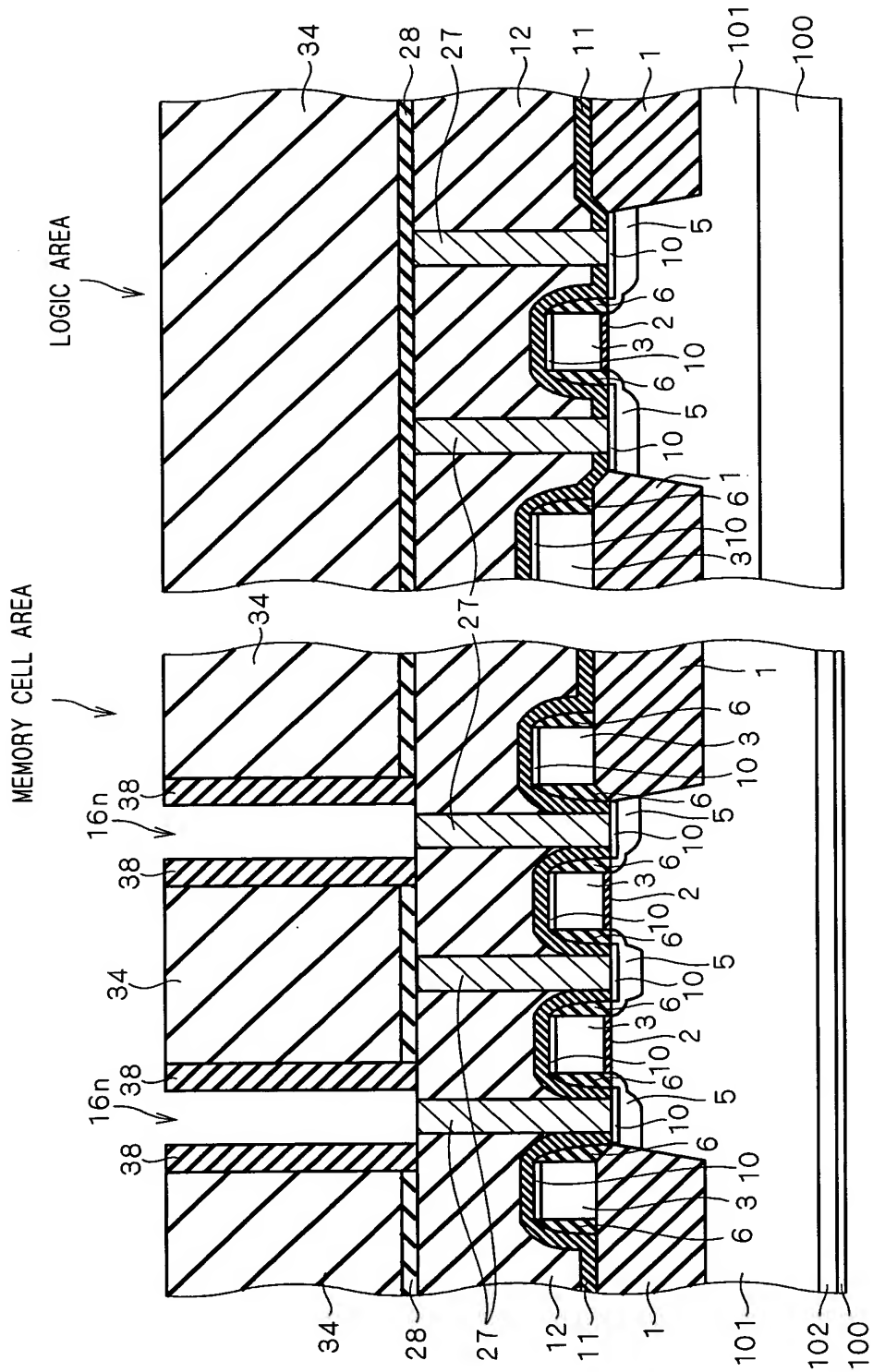


FIG. 83

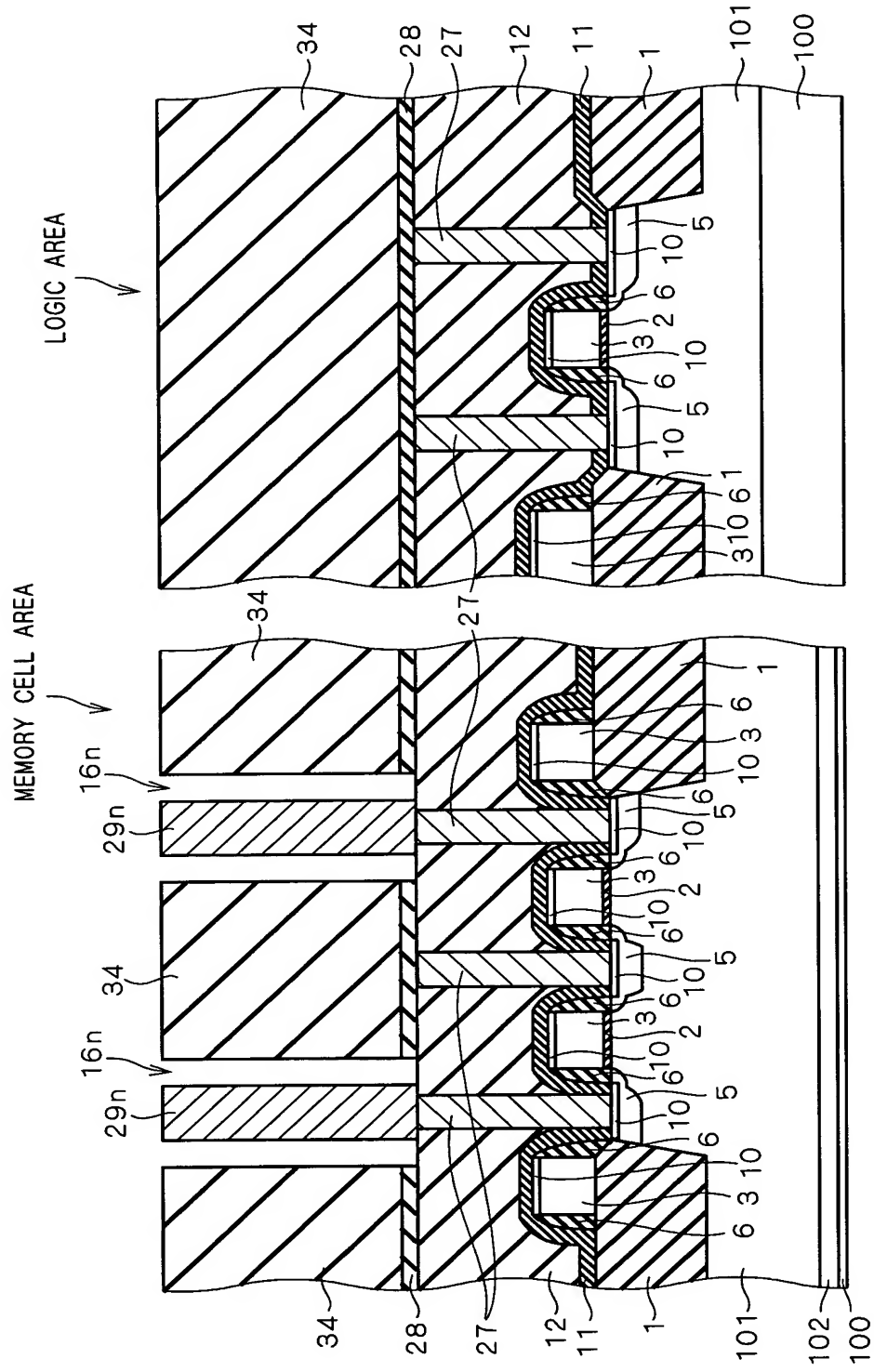


FIG. 84

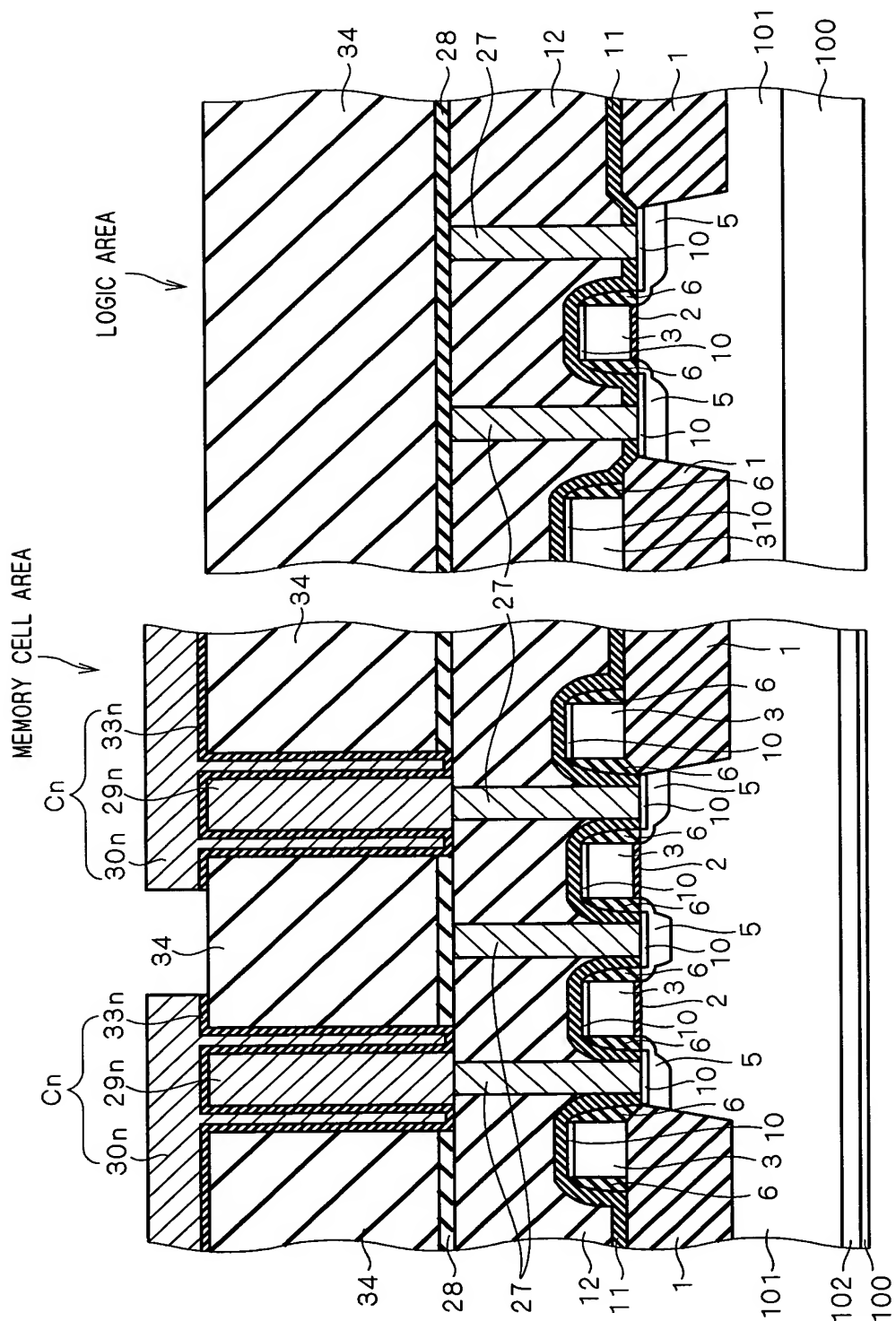
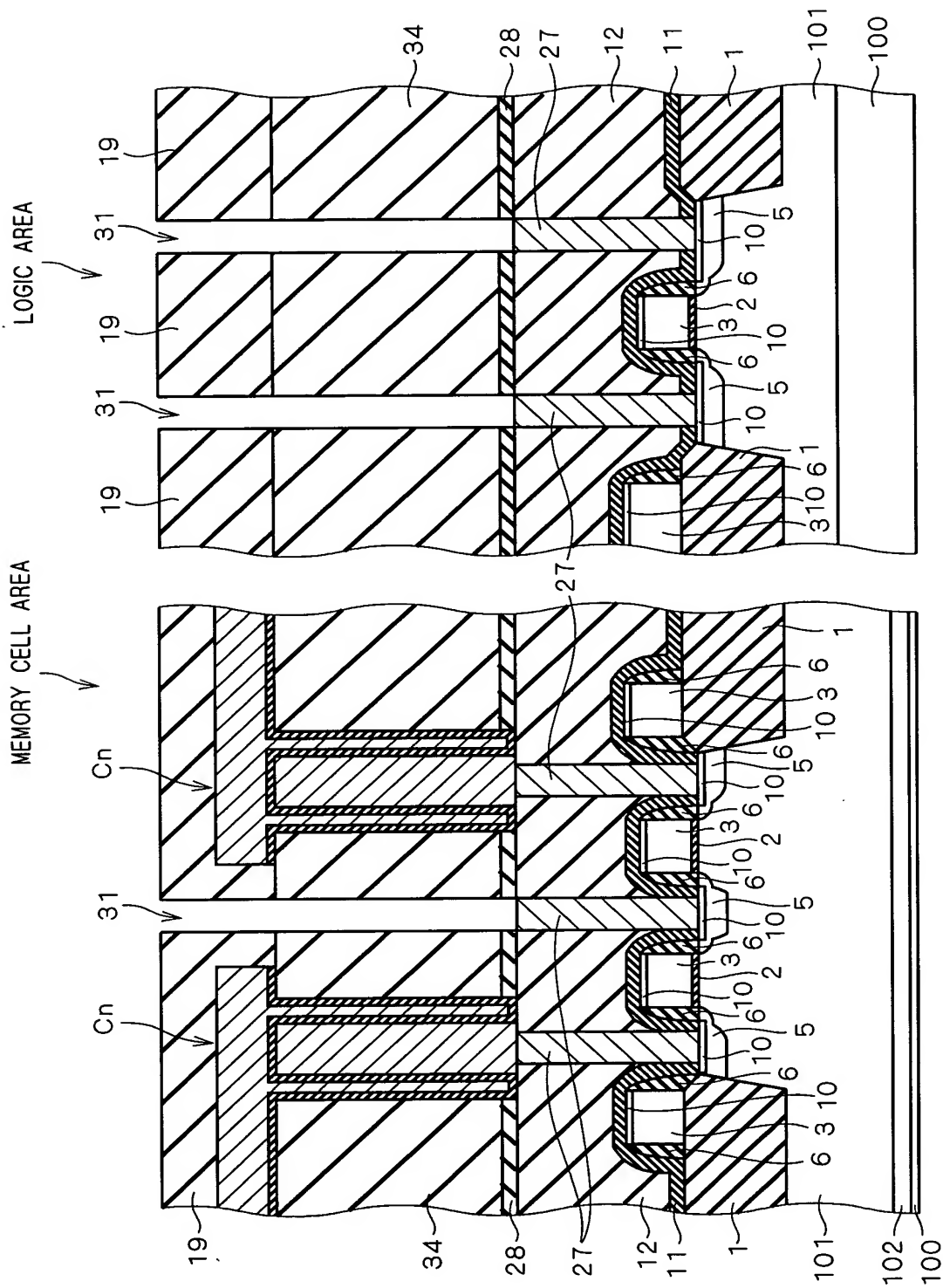
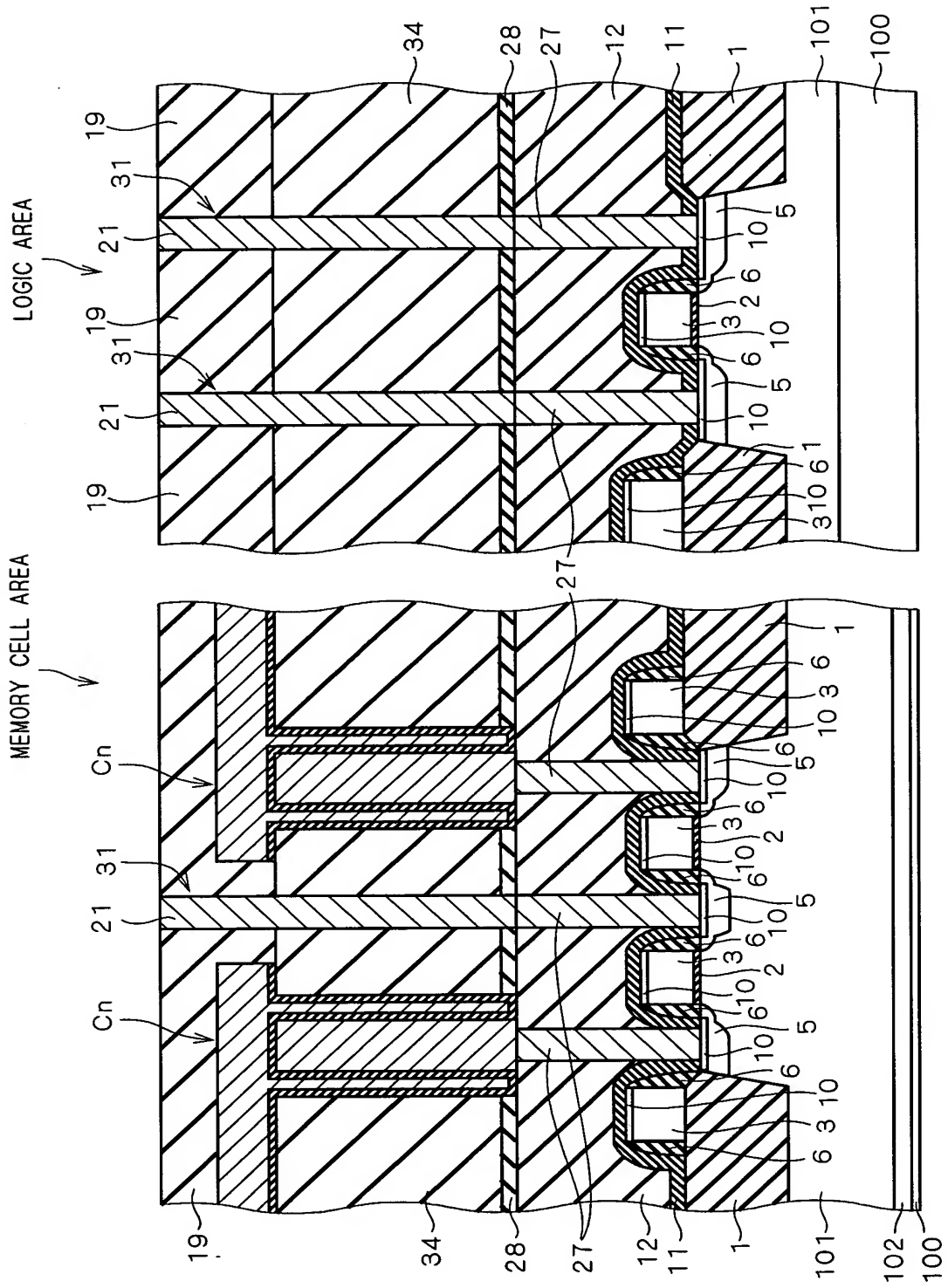


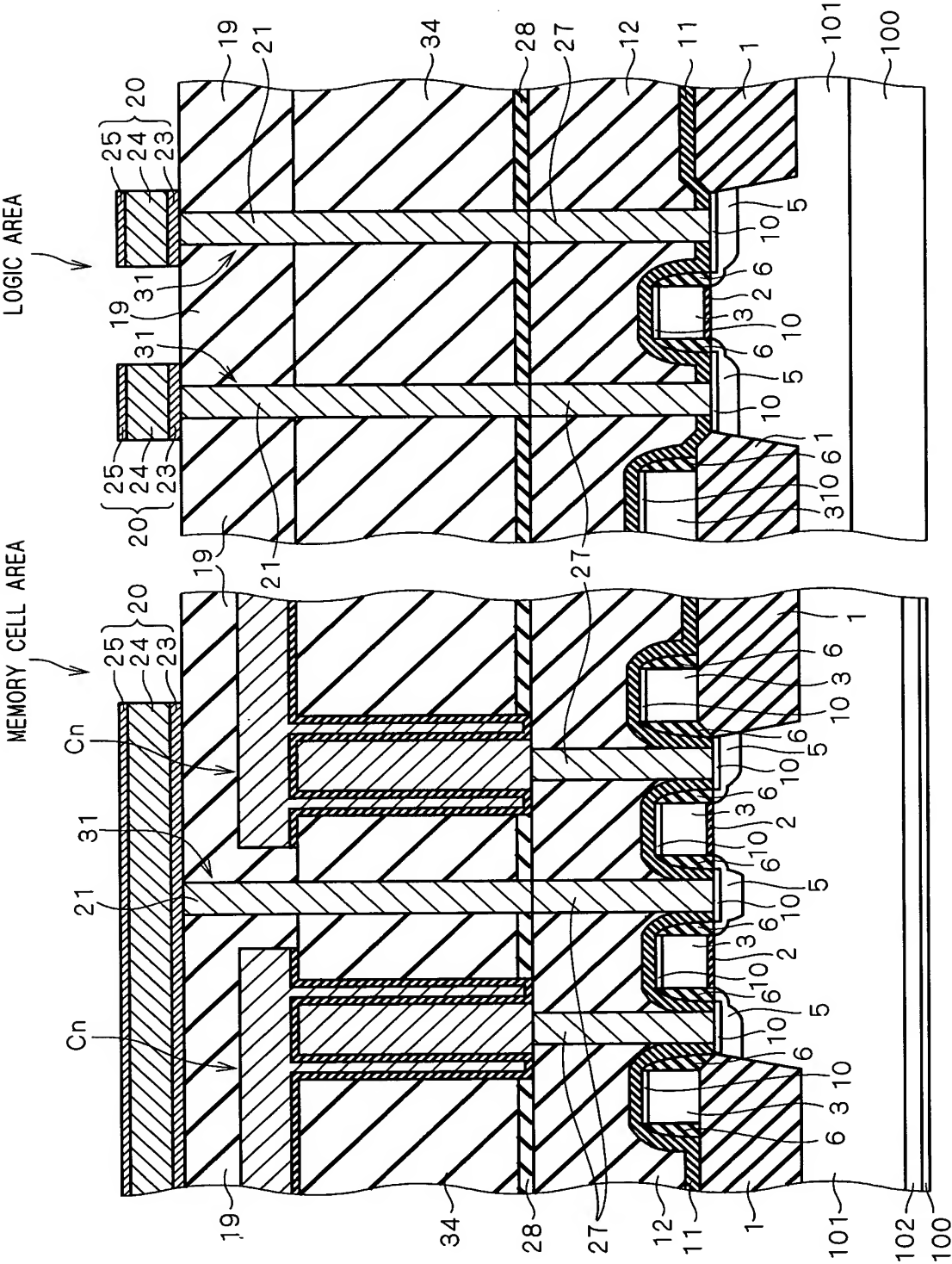
FIG. 85

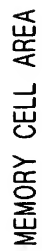


F I G . 8 6



F I G . 8 7





F I G . 8 9

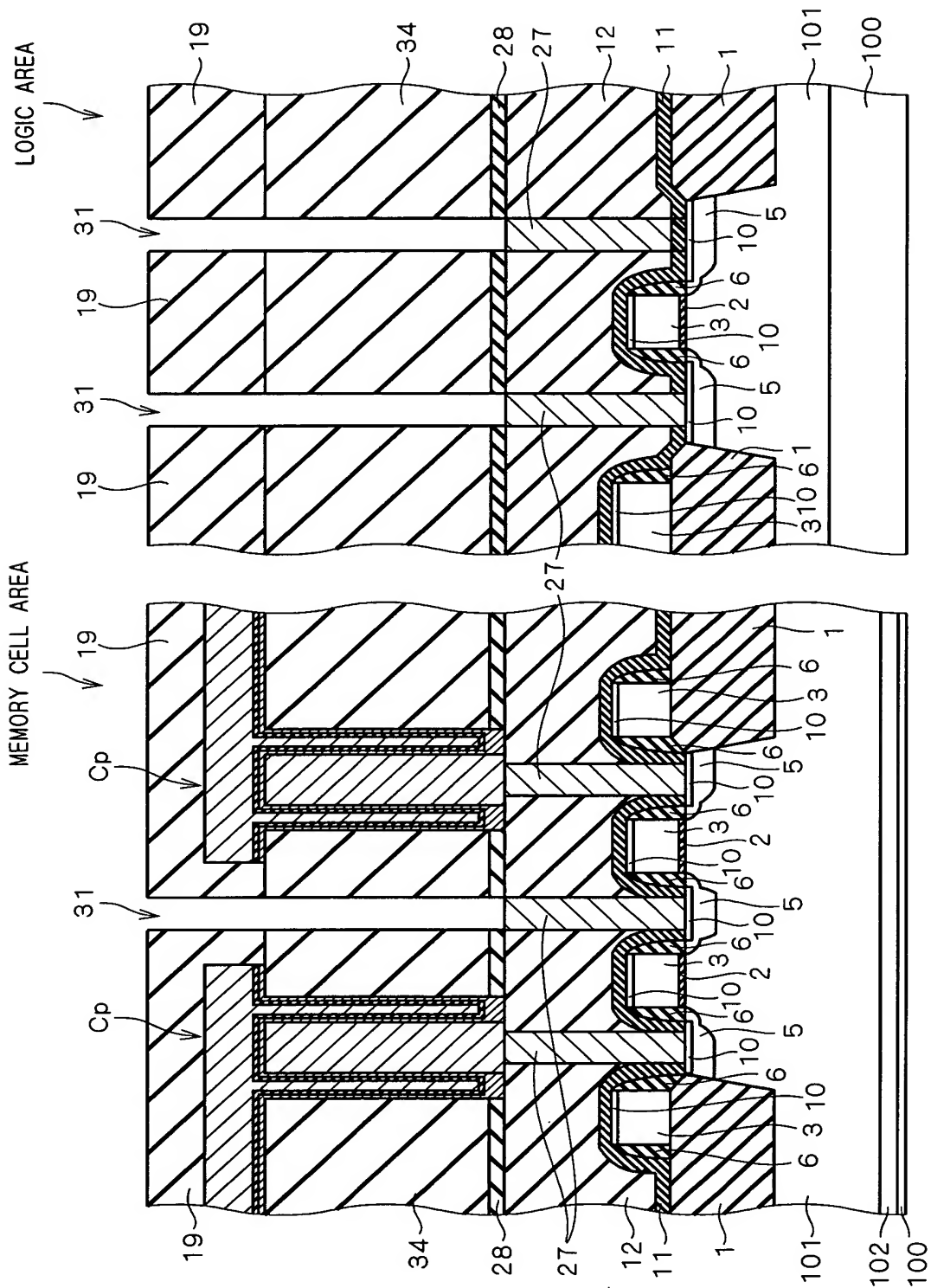


FIG. 90

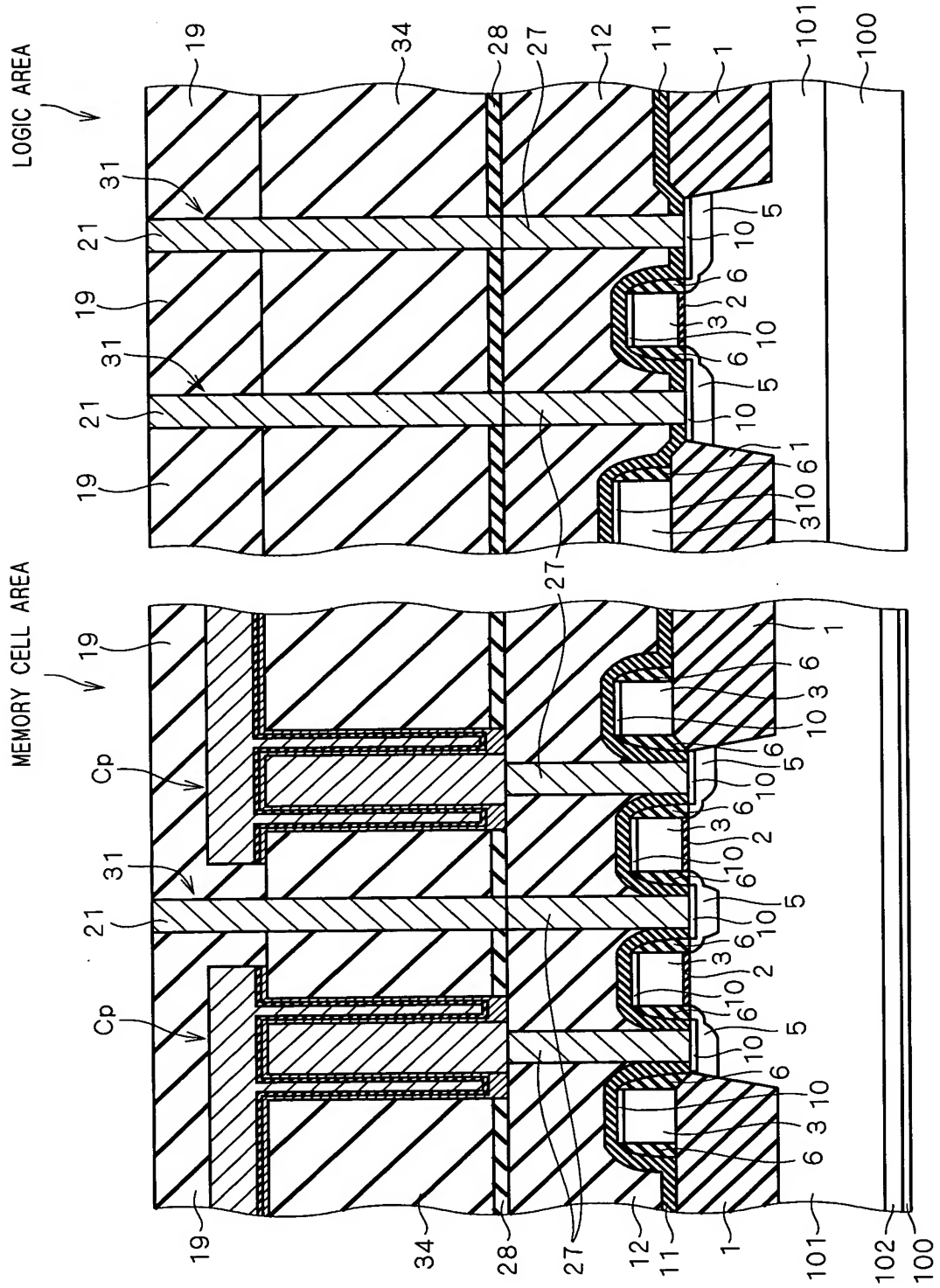
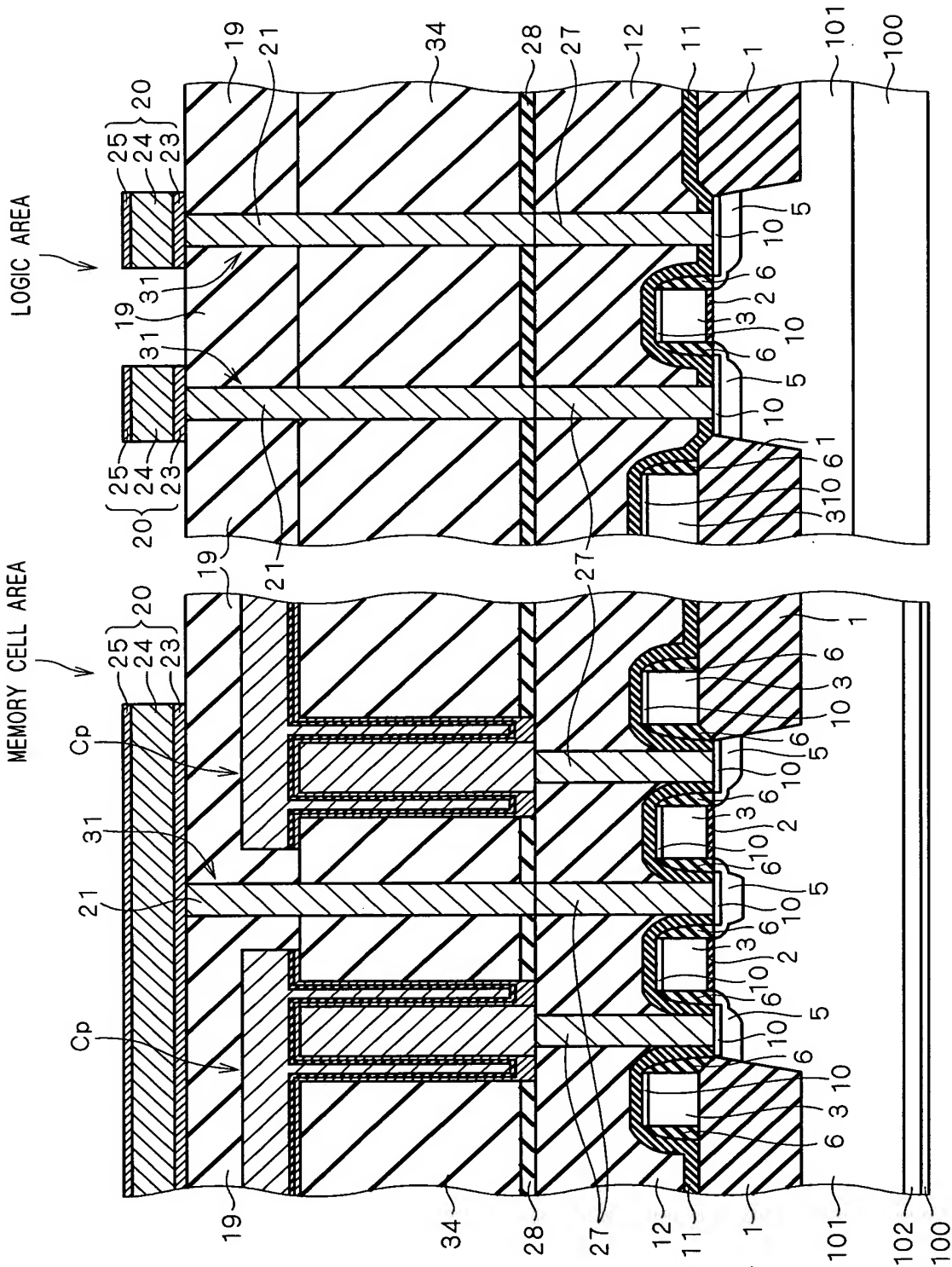
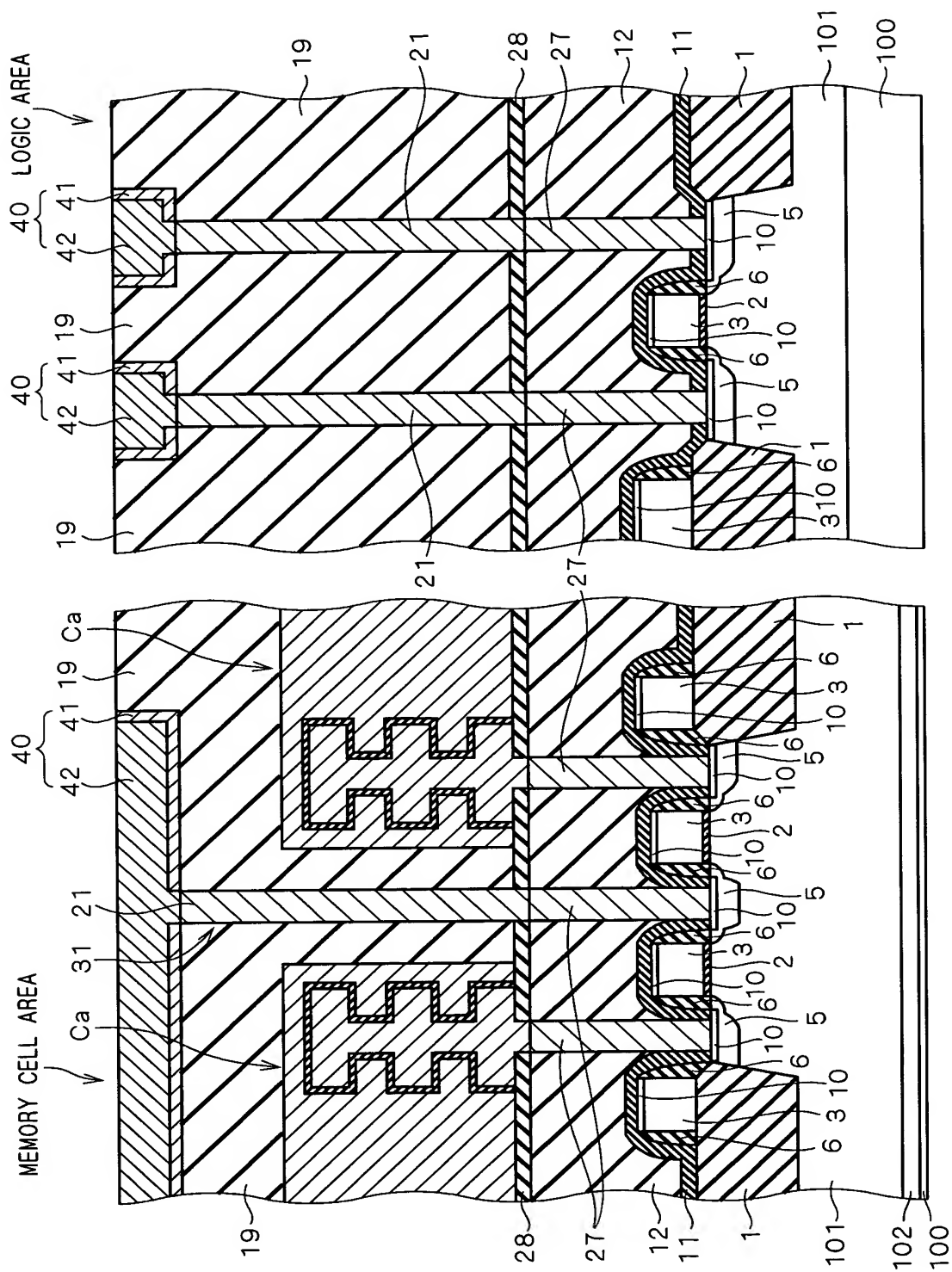


FIG. 91





F I G . 9 3

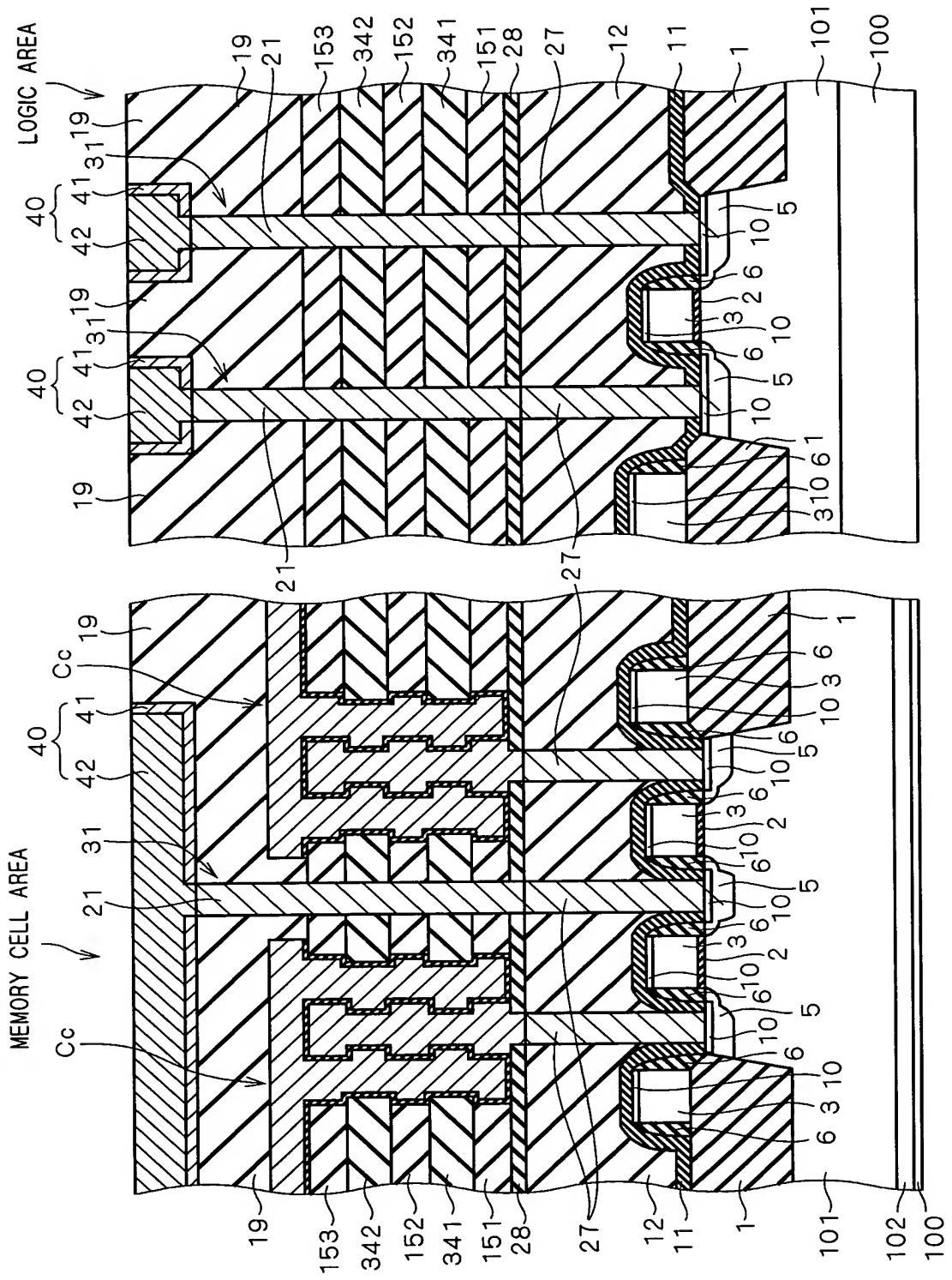


FIG. 94

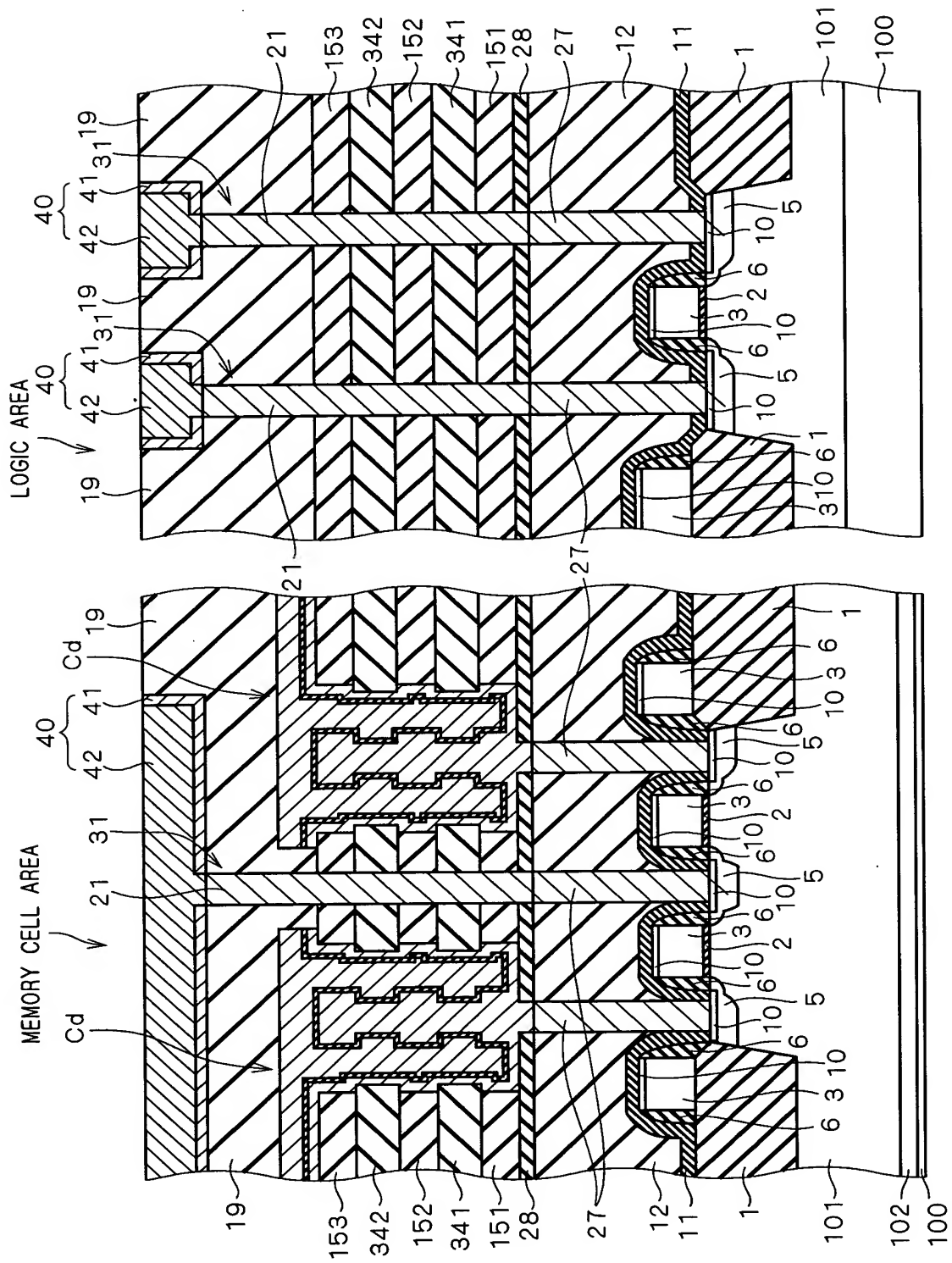
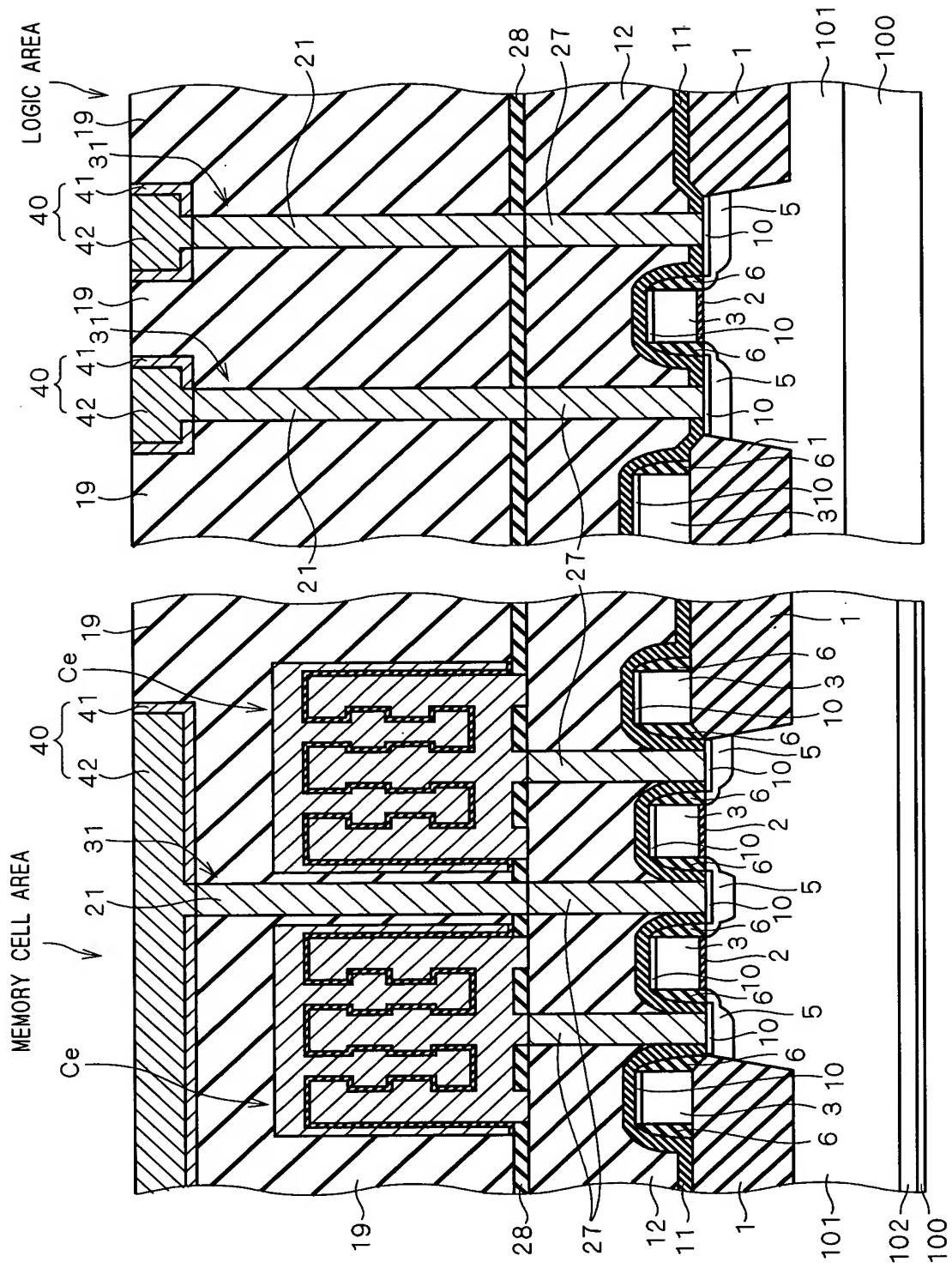
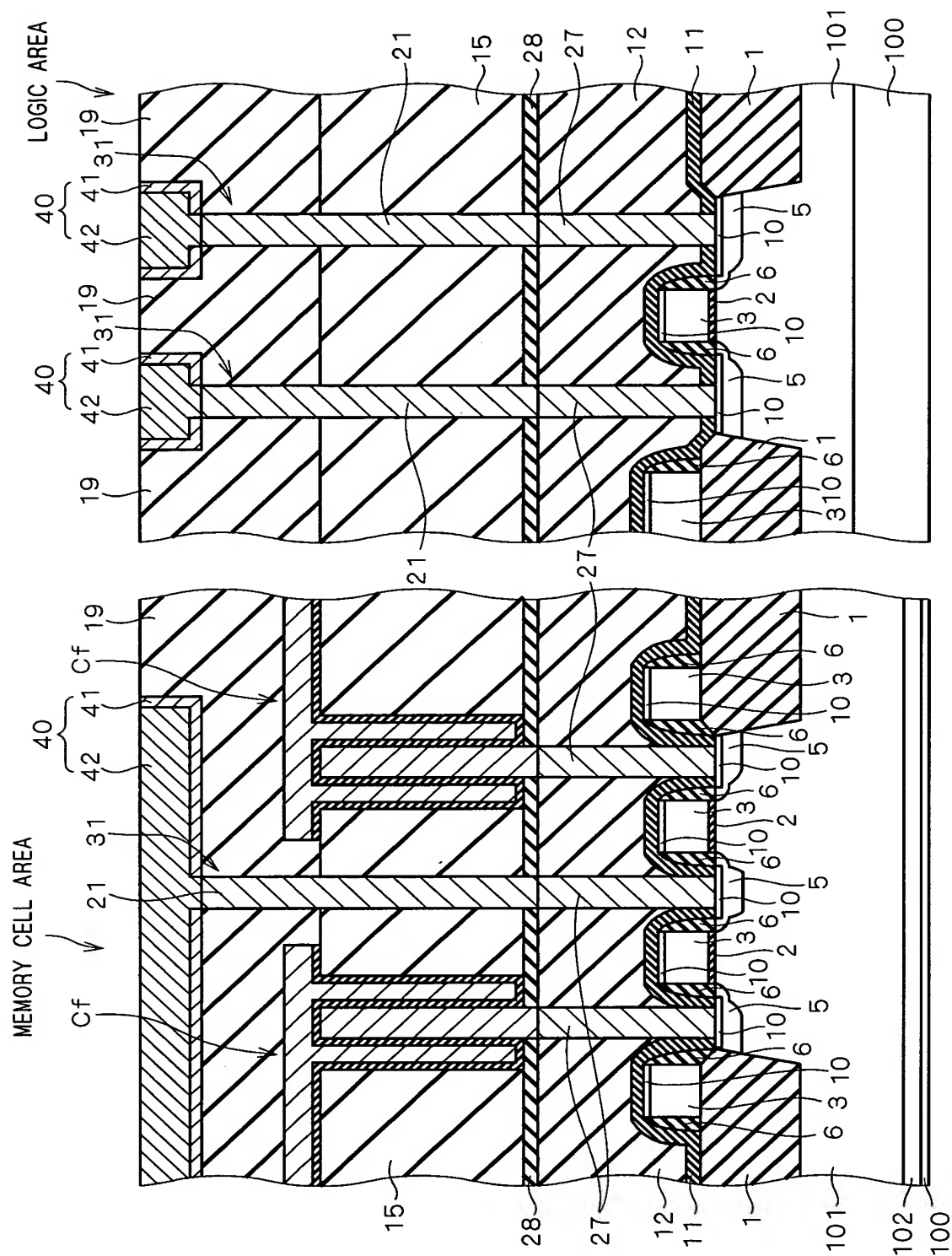
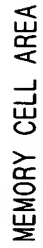


FIG. 95







F I G . 9 8

